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Compute Project

Open Accelerator Infrastructure (OAI) - Universal Baseboard (UBB)

Base Specification r2.0 v1.0

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2. Compliance with OCP Tenets

2.1. Openness

UBB Base Specification is an open standard with joint contribution across Hyperscalers, ODMs, component suppliers, and connector vendors.

2.2. Impact

UBB Base Specification defines common form factor compatible with Nvidia HGX Form Factor spec for AI/HPC accelerator modules and greatly cut down design cycle time and resources for companies to adopt the standard.

UBB Base Specification has been widely adopted by Hyperscalers, CSPs, and OEMs.

2.3. Scale

UBB supports total power consumption up to 12KW with multiple scale up and scale out topologies based on solution providers product definitions.

UBB supports industrial latest technologies with SerDes speed rate at 112G-PAM4 and cooling solutions.

2.4. Sustainability

UBB supports both air, liquid, or hybrid cooling for existing data center deployment and improve facility PUE and WUE when data center is equipped with full liquid cooling solution.

UBB is form factor compatible with Nvidia HGX baseboard. Single system design to support both solutions will reduce the time and cost of engineering development and resources.

3. Acknowledgements

We want to acknowledge all the OCP OAI Workstream members for their contributions to this specification: The incredible collaboration between customers, accelerator manufacturers, system developers, and industry partners shows how Open Compute develops industry-standard form factors and specifications that benefit all its members.

We would especially like to thank **AMD, Amphenol, Boyd, CoolerMaster, H3C, Intel, Intel Habana, Meta, Microchip, Molex, and Wiwynn** for their extra efforts in putting this specification together.

4. Introduction and Scope

Open Accelerator Infrastructure (OAI) is an initiative within the OCP Server Project to define a modular, interoperable architecture for systems targeting Machine Learning, Deep Learning, and High-Performance Computing workloads. OAI defines the logical and physical attributes of all the basic building blocks of an accelerator system design.

A standard way to connect this Open Accelerator Infrastructure to a CPU Box in a rack is shown in Figure1.

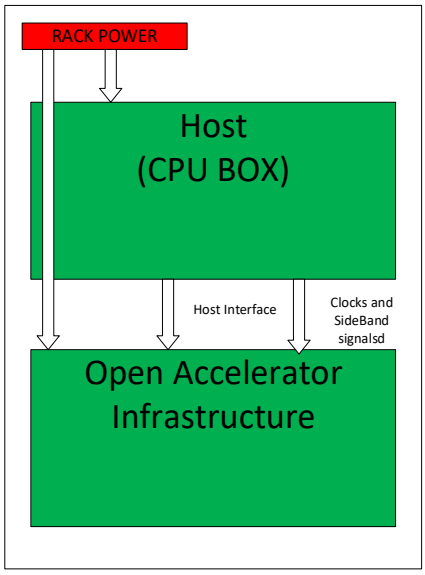


Figure 1 OAI as a disaggregated compute for AI in a Rack.

The Open Accelerator Infrastructure will be composed of these base building blocks:

- OAI Power Distribution (OAI-**PDB**): The translation between Rack Power to UBB module power needs.
- OAI Host Interface (OAI-**HIB**): The HIB provides the interface links between the UBB and head node(s).
- OAI Security, Control, and Management (OAI-**SCM**): This module provides OAI management, power sequencing, and security.
- OAI Universal Baseboard (OAI-**UBB**): The UBB Baseboard supports 8 OAM modules in various fabric and interconnects topologies.
- OCP Accelerator Module (OAI-**OAM**): Specification 1.0 defines the mezzanine module accelerator.
- OAI Expansion (Scale-out) Beyond UBB (OAI-**EXP**): Specifications describe connections between multiple OAI systems in the same rack or across different racks.

- OAI-**Tray:** The tray provides mechanical support to adapt various UBBs to both 19” and 21” Chassis and Racks
- OAI-**Chassis:** This chapter discusses both **air-cooled** and **liquid-cooled** implementations.

Specifications for each component will cover logic, power, mechanical, connector interfaces, and thermal infrastructure definitions to ensure interoperability between all the OAI elements.

These elements and their interactions are represented in Figure 2.

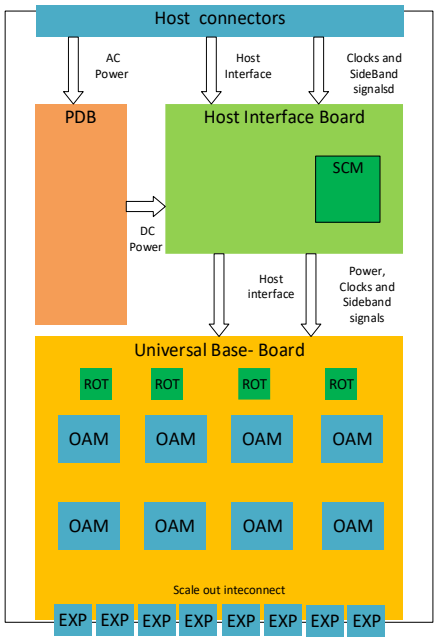


Figure 2 OAI building blocks

Figure 3 below shows an example of OAI system design by H3C as a composite of various OAI building blocks.

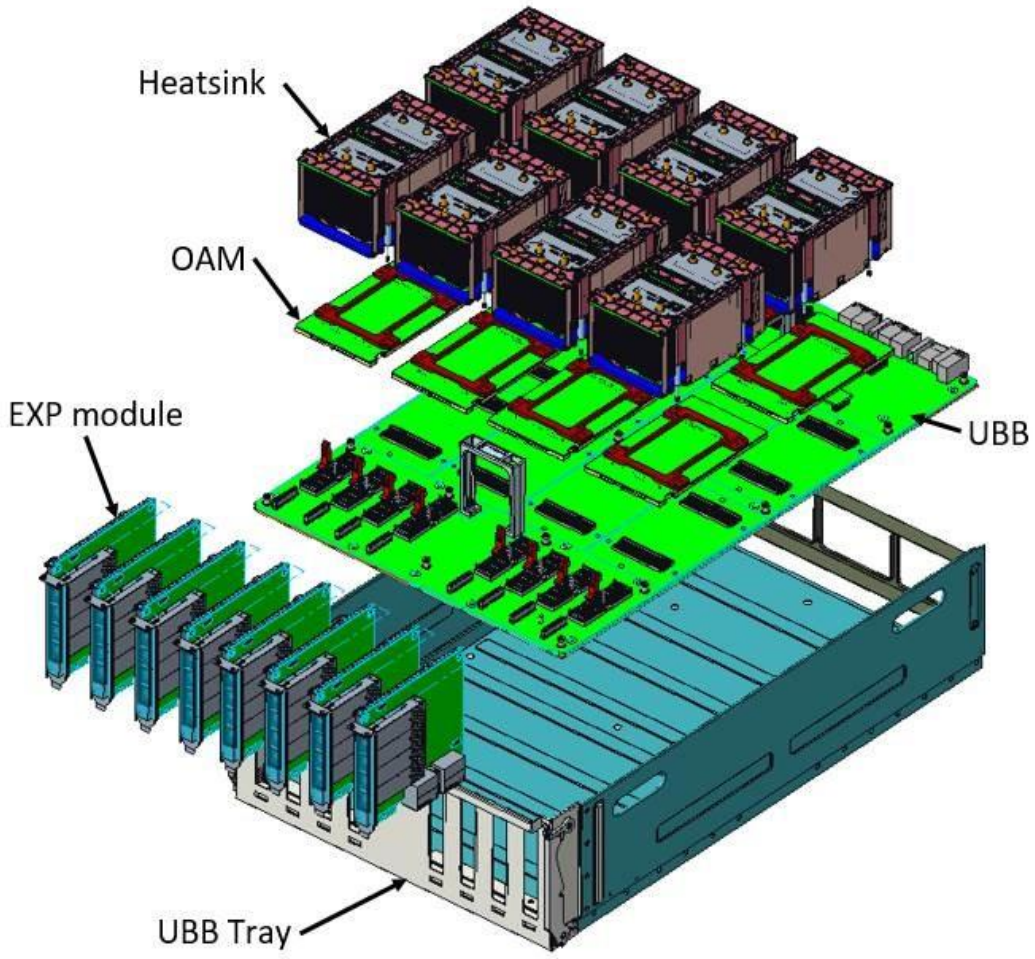


Figure 3 Example of OAI System Building Blocks

5. Universal Baseboard (OAI-UBB) High-level Description

The UBB is modular and flexible in supporting current and future OAM modules and providing maximum design flexibility for conceivable system designs. The UBB supports 8 OAM modules, but the board has been engineered to help comprehensive options of interconnecting fabrics and topologies, power domains, TDP's, cooling solutions, and scale-out options. While the board is optimized for a few standard configurations and released OAM modules, great care was taken to accommodate future trends and customer needs.

The Universal Based Board (UBB) is a building block that supports:

Table 1 Universal Based Board (UBB) Building Blocks

OAM Support	• Various interconnect topologies for 8x OAMs • Air or liquid cooling • OAM powered by 12V nominal up to 50W(optional) (*) • OAM powered by 54V/48V nominal up to 1000W (*) • One x16 host interface per OAM

Interface to HIB (Host Interface Board)	• 8 x16 connectors for host interface connections (one per OAM)
	  • Each Host Interface up to x16 lanes (for example, PCIe Gen5)
	  • Support for PCIe Gen5 and other future host interfaces
	• Power:54V/48V.
	• Sideband signals: I2C,PCIe2.0,USB2.0, Reset, Reference clocks, Power management, et al.

EXP Capabilities	• EXP modules for scale-out or switch-based interconnect** • Support QSFP-DD/OSFP • Power:54V/48V, 3.3V • Exposed from UBB to the exterior of the UBB Tray/System Chassis
Electrical Interoperability	• The current UBB reference design supports SERDES links up to 32 Gbps NRZ and up to 112 Gbps PAM4 • Two Micro USB connectors are exposed from the UBB to the exterior of the chassis for debugging (UART to USB)
Mechanical Interoperability	• PCB dimensions: 417mm wide x 655mm long • Supports both 19" and 21" rack chassis infrastructures • Defined mounting hole sizes and locations

Note:

* Different UBB designs may have different power support. Check UBB providers for specific product specification.

**Number of EXP is flexible, based on different UBB designs.

Figure 4 shows the major physical features of the UBB. Red lines show the power delivery connections to the OAMs. Yellow lines show the host interface, clock, and SCM signals to the OAMs.

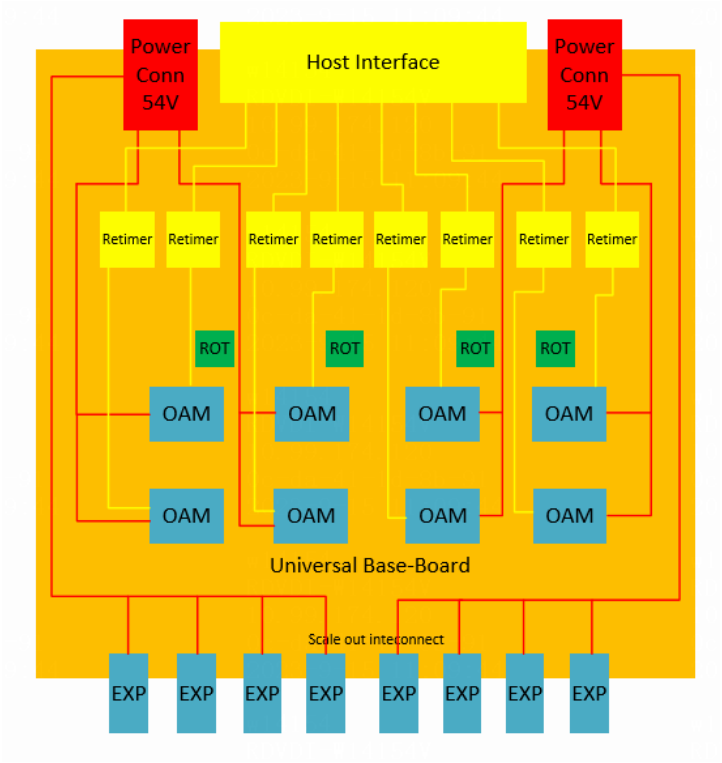


Figure 4 Example of UBB System Building Blocks

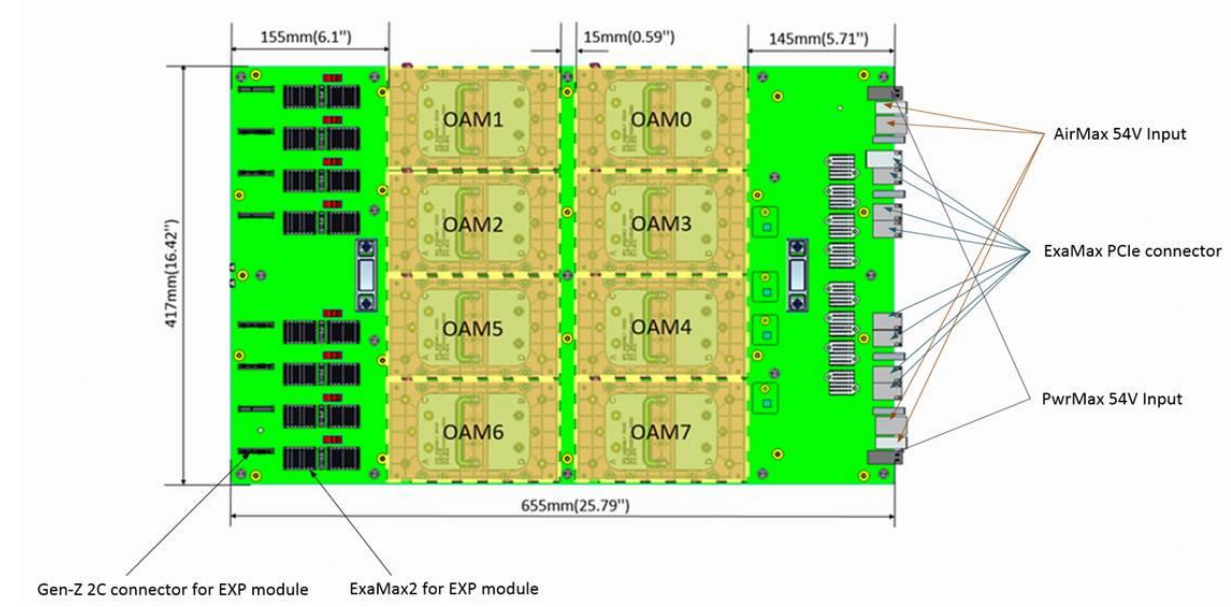


Figure 5 Universal Base Board (UBB)

6. Input and Output Interfaces

The UBB is the carrier board that populated with 8 OAM modules, and there are five primary interfaces to other boards in a complete system design:

1 OAM Interface: Interface to OAMs.
2 Host Fabric interface: Required interface to host(s) via PCIe or other host fabric. The interface fabric is routed to the Host Interface Board where it connects to either a host node integrated within the same chassis or a disaggregated host node.
3 EXP interface: Interface to the Expansion modules. EXP allows multiple OAMs to connect through OSFP/QSFP-DD connectors to external switches or node-to-node.
4 RoT Interface: Interface to the security module RoT.
5 Miscellaneous Signal Interface: SMBus, USB, Clocks, sideband signals provided by the Host Interface board.
6 Input Power Interface – 54V/48V inputs to the UBB.

6.1. OAM Interconnect Interface

As outlined in the OAM base specification, each OAM has up to eight x16 interconnect links. Each OAM to OAM connection can support different interconnect topologies based on number of links supported by the specific OAM populated on the UBB.

Refer to Section 7 for more details on the supported UBB interconnect topologies and OAM Base Specification for pin-out and others information.

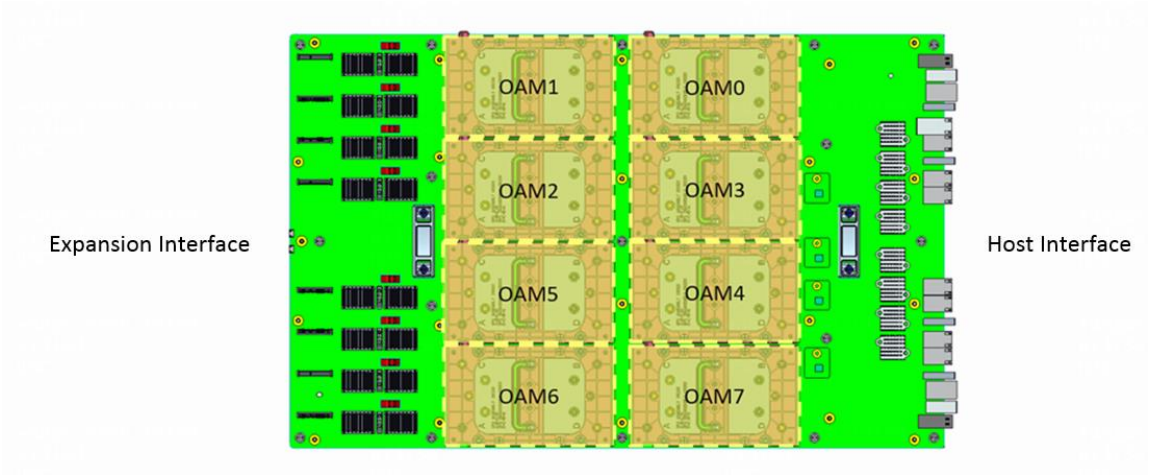


Figure 6 UBB Host and Expansion (scale-out) Interfaces

6.2. Host Fabric Interface

This section describes the host interface to the HIB board, including supported fabrics and speeds.

6.2.1. Host Interface: High-speed interface

There are eight x16 SerDes links dedicated for host interface connections. Each OAM module on the UBB routes an x16 link to a dedicated ExaMax connector (shown in Figure 5) which connects to the Host Interface Board.

Different implementations of the Host Interface Board provide customized topologies that allow the UBB to interface to a single host node or multiple hosts in various configurations. System design can also support either integrated head nodes in the same chassis as the UBB or disaggregated head nodes, which cable to a separate UBB chassis within the rack.

The specification supports industry-standard host protocols such as PCIe Gen5, CXL, Infinity Fabric, and other alternate protocols. The UBB has space allocated for re-timers that may be needed to support specific protocols or configurations needed with different OAM and system designs.

6.2.2. Pin list

A detailed pinout please refer to *OAI-UBB_Pinlist_r2.0_v1.0.xlsx.*

6.3. EXP interface

The UBB supports 8x EXP modules with each EXP module supports 4x QFSP-DD/OSFP connectors for scale-out topologies that connect multiple UBB boards or external switches through high-speed DAC or optical cables. The number of EXP modules and QSFP-DD/OSFP connectors varies based on different designs.

6.3.1. High-speed support

The QSFP-DD/OSFP connectors are exposed to external connection of the UBB tray to support connection to other UBB systems or switches. The QSFP-DD/OSFP links can be connected through external DAC or optical cables.

OAI UBB reference board supports SerDes data rates up to 112Gbps PAM4. In addition, to support future configurations, space for re-timers has been allocated in the EXP module to support various system and cable configurations.

6.3.2. I3C/I2C/SPI/MDIO/JTAG

An I3C/I2C interface is defined on each EXP module to enable cable management and FRU access with either to be managed by OAM or BMC. SPI, MDIO, JTAG is also supported in the EXP module.

6.4. Miscellaneous Signal Interface

The UBB supports additional side band signals from the host interface board for security, control, and board management.

6.4.1. Clock and I3C/I2C Signals

The UBB receives its primary clock, AUX clock, downstream clock from the HIB.

6.4.2. Board management

There are I3C/I2C, PCIe2.0, for UBB management.

- I3C/I2C is used to read OAM information, status, and UBB FRU.

- The host node controls OAM Reset through HIB to UBB CPLD.
- PCIe2.0 is used for transferring data from FPGA to BMC.

6.4.3. Power management

There are PWREN, PWROK, PWRBRK#, Thermtrip# signals for power management.

- PWREN: UBB power ready assert OAM power enable.
- PWROK: Indicates OAM power is stable and asserts PWROK to CPLD
- PWRBRK#: There are two sources to trigger PWRBRK#. One is from BMC, and the other is from PSU alert
- Thermtrip#: it indicates OAM silicon has reached an elevated temperature. OAM will power off itself when Thermtrip# is triggered. UBB may or may not shut down the entire board depending on system design requirements.
- UBB Power Ready (UBB_PWR_READY): Assert UBB_PWR_READY to notice BMC on HIB interface when all UBB powers are ready.

6.5. Input Power Interface

UBB only supplies single 54V/48V to support OAM TDP up to 1000W. A group of connectors supplies 54V/48V DC Power to UBB through HIB interfaces.

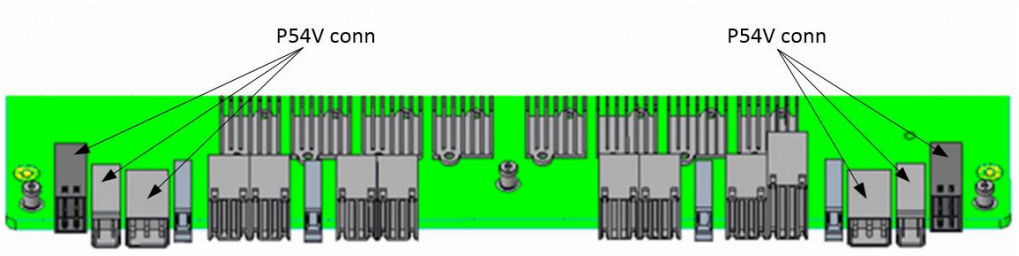


Figure 7 Input Power connectors Placement

There are six dedicated 54V/48V connectors delivering power from the HIB to the UBB.

UBB is designed to support different rack infrastructures and form factors and interface to different system-specific HIB and PDB implementations that support bus bar or discrete power supply solutions. A typical implement is below:

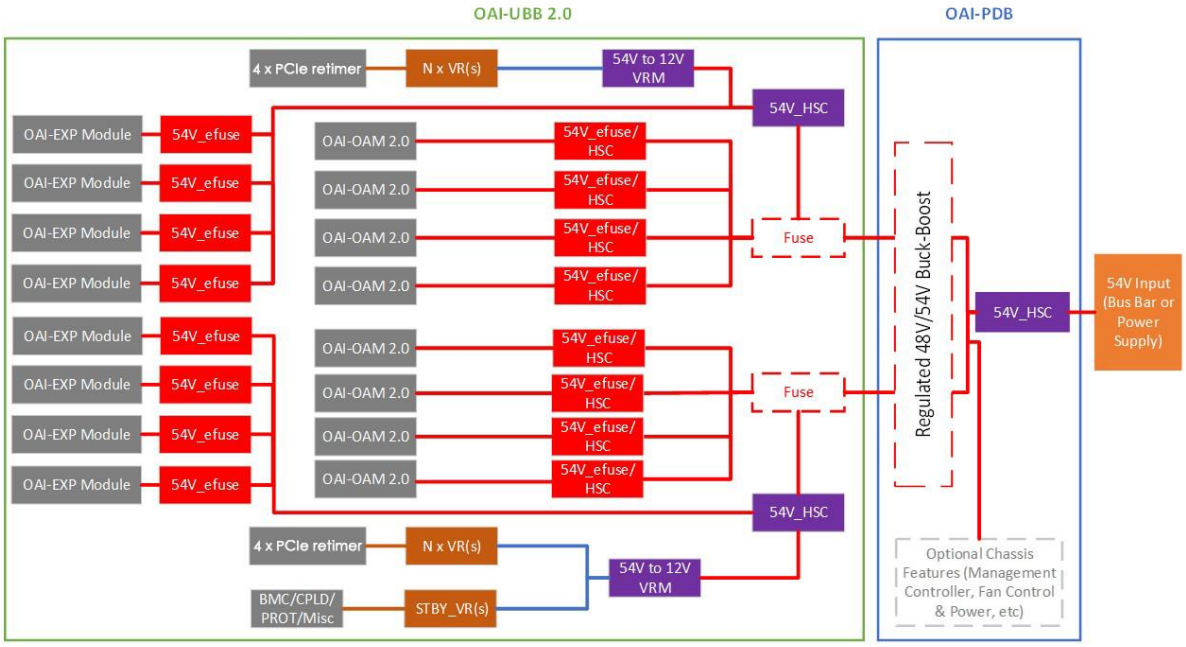


Figure 8 OAI Reference UBB power Delivery Diagram

6.5.1. UBB System Power

UBB is part of the OAI system infrastructure, which supports two distinct power architectures.

One is centralized power in the rack with a busbar, often energized by an in-rack power shelf with several 54V/48V PSUs.

The other method utilizes PSUs integrated into the individual OAI system chassis itself. The PSU's input is from an AC supply, and its output is 54V. For example, 54V 4000W Platinum PSUs with 3+3 redundancy is one known OAI system implementation.

6.5.2. 54V/48V based OAM power input

Each OAM has an isolated source from 54V/48V through a dedicated hot-swap controller. The system provider who designs the OAI system shall implement bulk capacitors to support OAM 54V/48V power rails to support OAM EDP. The implementation shall be on the HIB power connectors' side. Refer to section 5.5.4 for detailed excursion power support.

The following table summarizes the voltage range UBB supports.

Table 2 UBB input voltage range

	Minimum	Nominal	Maximum
Operating voltage	40.0V	48.0/54.0V	59.5V

The recommended range includes DC level, noise, and other transients. The input rails must remain within 40 to 59.5v. Although specific UBB has a particular OAM TDP support target based on design, UBB

could support up to 1000W TDP OAM. The continuous current specification for nominal input voltages between 48.0V and 54.0V can use linear interpolation to approximate.

Table 3 UBB(up to 1000W OAM) input continuous current specifications

Specification	Voltage(nominal)	Maximum Value	Moving Average
Input 54V	54.0V	222.2A	continuous
Input 48V	48.0V	250.0A	continuous
Total baseboard power	48.0V to 54.0V	12000W	continuous

UBB system provider shall check with OAM vendor to get detailed excursion support requirements and apply design accordingly. OAI UBB reference boards support OAM's excursion design power (EDP) of 1.75x TDP (1000W based on 48/54V) for a 2ms duration.

Table 4 UBB(up to 1000W OAM) EDP support example

Voltage	EDP	Current *	Duration
54V or 48V	2x TDP	200%*222.2A(or 250.0A)	<= 20us
	1.75x TDP	160%*222.2A(or 250.0A)	<= 2ms
	1.5x TDP	150%* 222.2A(or 250.0A)	<= 5ms
	1.25x TDP	120%*222.2A(or 250.0A)	<= 10ms
	1.1x TDP	110%*222.2A(or 250.0A)	<= 20ms

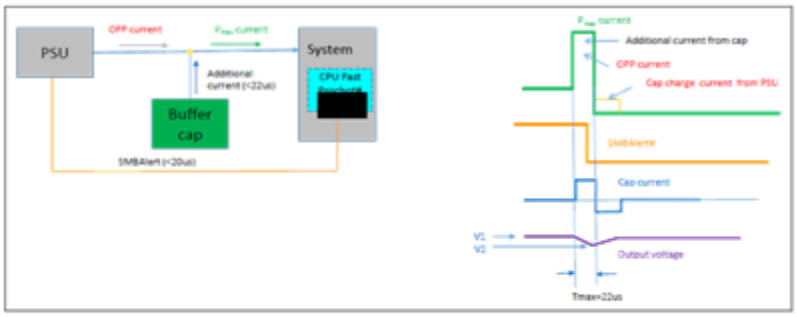
6.5.3. 12V based OAM Power input

The 12V input is only 50W optional for OAM components except GPU/ASIC

6.5.4. OAM Excursion Power Support

This section describes the 54V power design guide based on the UBB reference system.

The figure below for reference is based on the peak current requirement to calculate Cmin capacitance for the microsecond(us).



The total required Min buffer capacitance to support P_{max} can be calculated as follows:

$$C_{\min}(\mu F) = 2 \times (P_{\max} - P_{opp}) \cdot \frac{T_{\max}(\mu s)}{V^2{}_1 - V^2{}_2}$$

Figure 9 Cmin calculation for OAM peak current

- Cmin: Min buffer cap size assuming PSU(s) has 0uF output capacitance and 0uF on the baseboard power rail.
- Pmax: the max system power due to CPU Pmax virus condition.
- Popp: the PSU minimum OPP power level, and it is always set above system power budget corresponding with CPU's Pmax.app
- Tmax: the throttle time delay after the system power exceeds the pre-defined power threshold.
- V1 and V2: The PSU output voltage levels at the beginning and the end of the Pmax time interval (Tmax)

The table is an example for 54V power at 2x EDP 20us calculation result based on reference UBB design. The 54V OAM 1000W EDP with 20us duration is about 94uF of Cmin. The designer should trade off your PCB space and cost to provide a VR/Cap solution for peak power requirements.

Table 5 Cmin requirement at 2x EDP 20us

	1000W EDP / 54V OAM
Cmin(uF)=	94
P_EDP(2x TDP)(W)=	2000
P_TDP(W)=	1000
Tmax(us)=	20
V1(54V_Busbar Vmin spec,-10%)(V)=	48.6
V2(OAM Vmin spec)(V)=	44

6.6. 40V ~ 59.5V power layout guidance

Manufacturing defects can result in shorts or faults across large voltage differentials. This risk needs to address due to the high voltages on the UBB.

Industry safety standards (IEC CDV 62368) require additional safeguards (i.e., creepage/ clearance distances, access restrictions, et al.) for systems with voltages that exceed 60V. Voltage differentials of

less than 60Vdc are classified as ES1 voltage sources. While ES1 systems do not require explicit safety safeguards, the guidelines below will minimize the risk of a fault that could cause high energy dissipation or fire.

Table 6 40V ~ 59.5V layout guidance

Layout Recommendations before Hot Swap Controller / Fuse	**Minimum spacing between conductors with high potential differences >40V**
Internal Layer	25 mils (0.64mm)
External Layer	120 mils (3.0mm)
Z-Axis	17 mils (0.43mm) spacing or 3-ply prepreg
Layout Recommendations after Hot Swap Controller / Fuse	**Minimum spacing between conductors with high potential differences >40V**
Internal Layer	25 mils (0.64mm)
External Layer	60 mils (1.5mm)
Z-Axis	3 mils (0.076mm)

Exceptions may be necessary due to the inherent spacing of components and should use DFMEA to evaluate thoroughly on a case-by-case basis.

Good power and ground isolation for an external layer on the UBB are below.

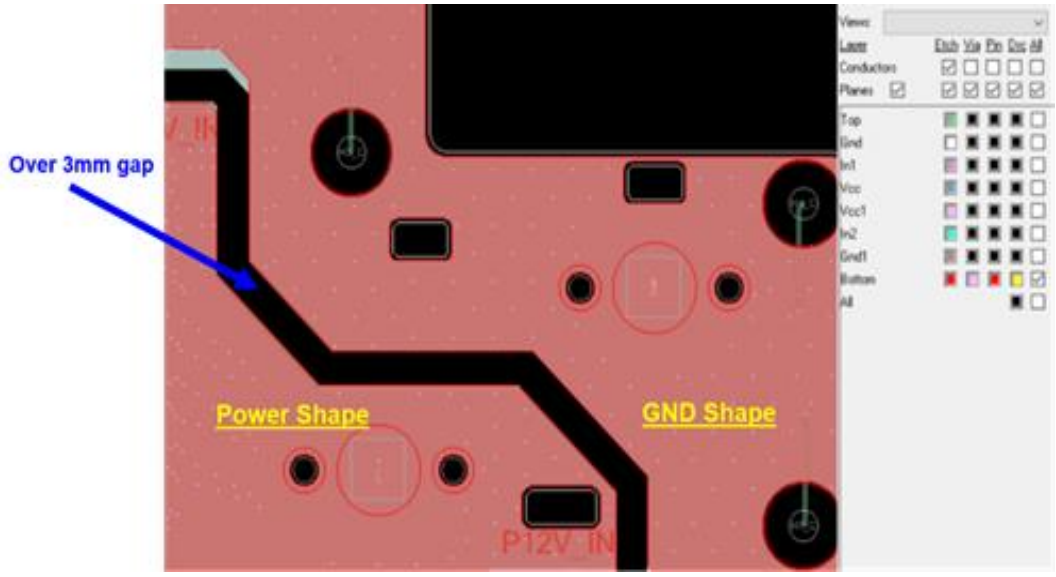


Figure 10 power and GND isolation

7. UBB Electrical Specification

This chapter describes details of the UBB electrical design.

7.1. Board Architecture specification

The OAI-UBB boards will share a standard hardware architecture definition for various design areas such as Clock distribution, Power Sequence Control, Telemetry, I2C, and GPIO assignments. The standard hardware specification intends to have a single Firmware and Software definition that can cover all different designs and to re-use the hardware solutions as much as possible across the other products. The typical hardware architecture components include the following definitions.

- Power Delivery
- Clock Distribution
- I2C Interconnectivity
- Power and Reset control
- Power and Reset Sequence
- GPIO definition

7.1.1. System Clock Architecture

Host to HIB will run in SRIS mode. HIB to UBB will be standard clock mode. SRIS also supports Spread-Spectrum Clocking (SSC) for EMC/ EMI. For 112G SerDes link, OAM and EXP local clock is recommended. When EXP module is in PCIe NIC configuration,100M clock can be supplied by OAM or UBB depending on the application.

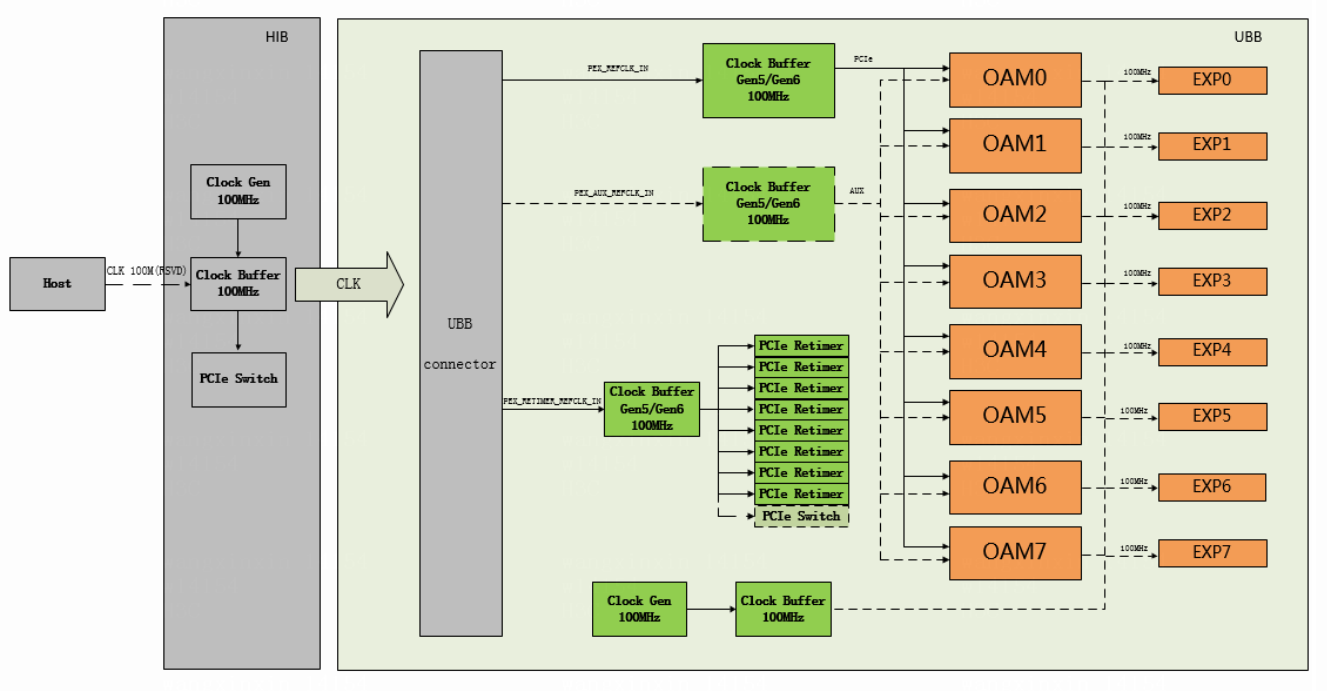


Figure 11 OAI Reference UBB clock diagram

7.1.2. I3C/I2C architecture

There are two I3C/I2C buses from HIB interface, as illustrated in figure12 below.

There's one FRU EEPROM on the UBB board to be accessed through BMC.

Below is UBB I3C/I2C pull-up resistor value calculation. Each board design has to get the pull-up resistance value based on the design requirement.

The minimum resistance calculation as

$$R_p(min)=(V_{cc}-V_{OL}(max))/I_{OL}$$

V_{cc} is the bus voltage, $V_{OL}(max)$ is the maximum voltage that can read as logic-low, and the maximum current that the pins can sink when at or below V_{OL}.

The maximum resistance calculation as:

$$R_p(max)=t_T/(0.8473xC_b)$$

t_T is the maximum allowed rise time of the bus, and C_b is the total bus capacitance.

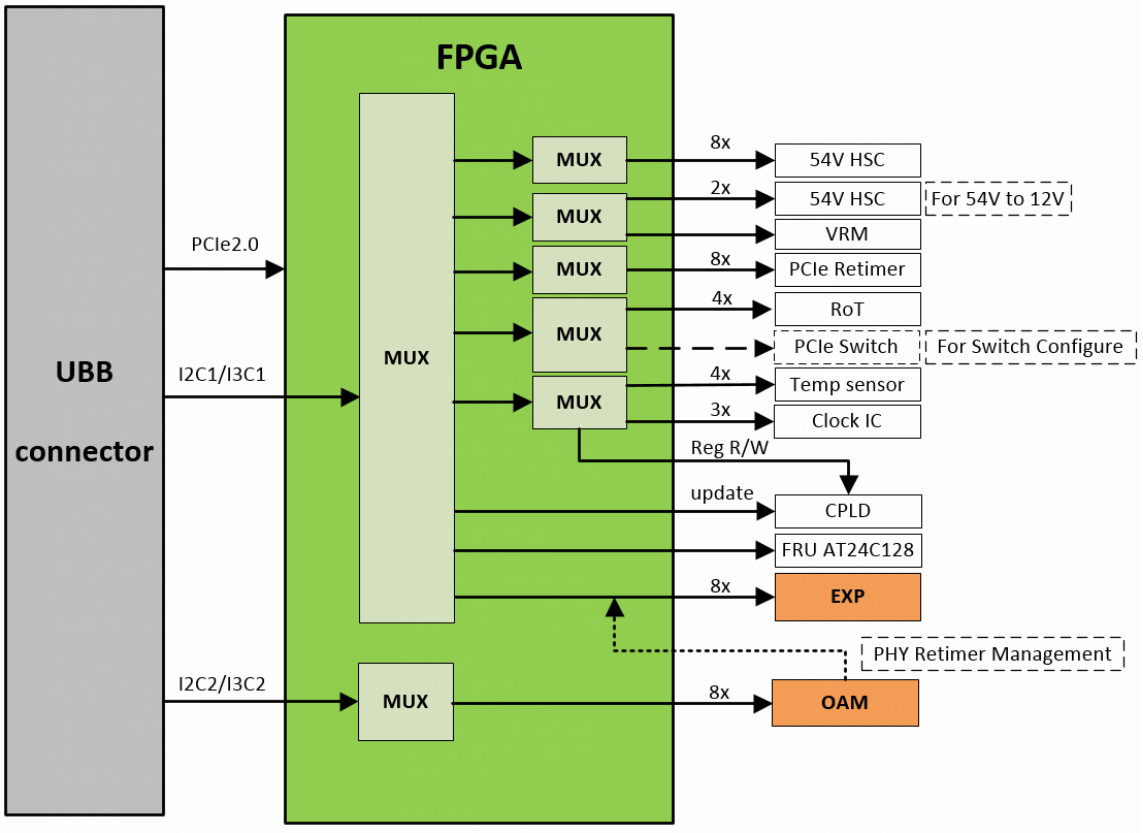


Figure 12 I3C/I2C/SMBus Block Diagram

7.1.3. Power control

The UBB provides 54V/48V to 8x OAMs. And the 54V/48V power is directly connected from the HIB power connector (P54V_0, P54V_1, P54V_2, P54V_3, P54V_4and P54V_5).

The management device of HIB controls all voltage power on/off through the I3C/I2C bus to CPLD. The UBB provides 400W (8x 50W) over 12V rail, 8000W (8x1000W) over 54V/48V rail for OAMs and provides 3200W over 54V/48V rail for EXP. Power sequence and management on UBB is managed by CPLD based on system design implementation.

7.1.4. Reset

Figure 13 below shows UBB reset diagram from the HIB management device (ex, BMC) to UBB. All UBB components reset can be controlled by HIB I3C/I2C interface through UBB CPLD.

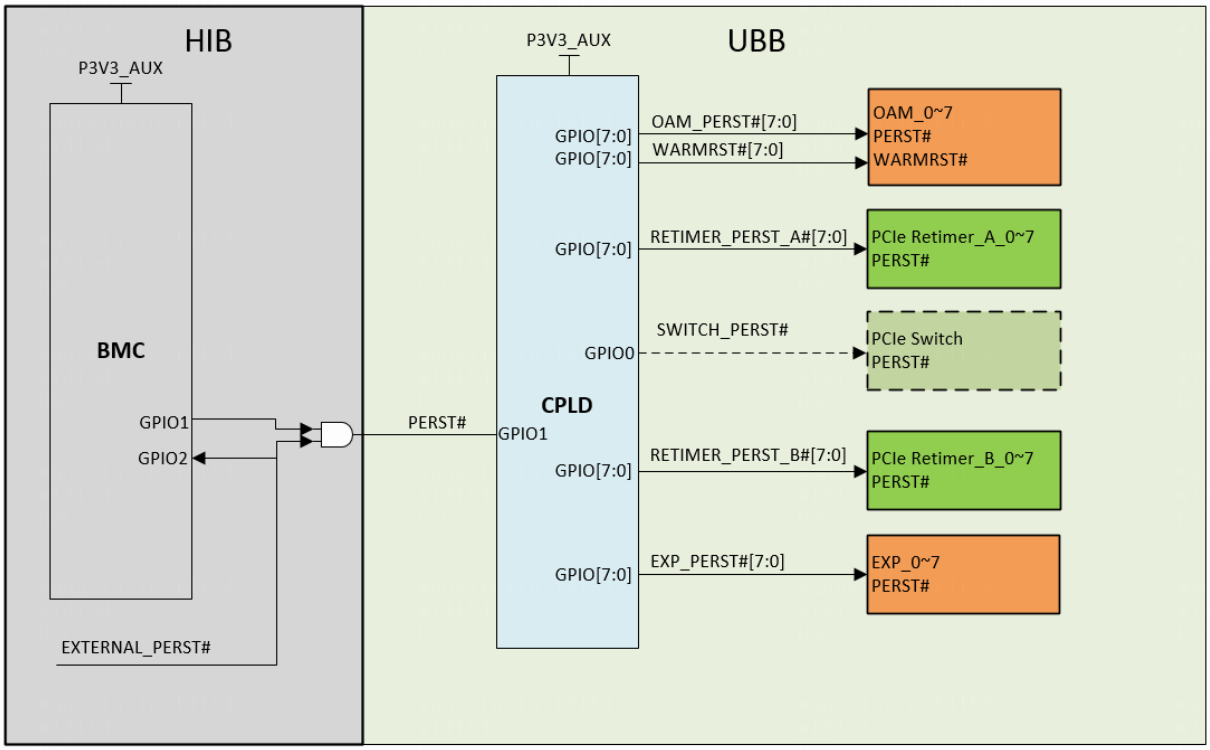


Figure 13 UBB Reset signals diagram

7.1.5. Power Diagram

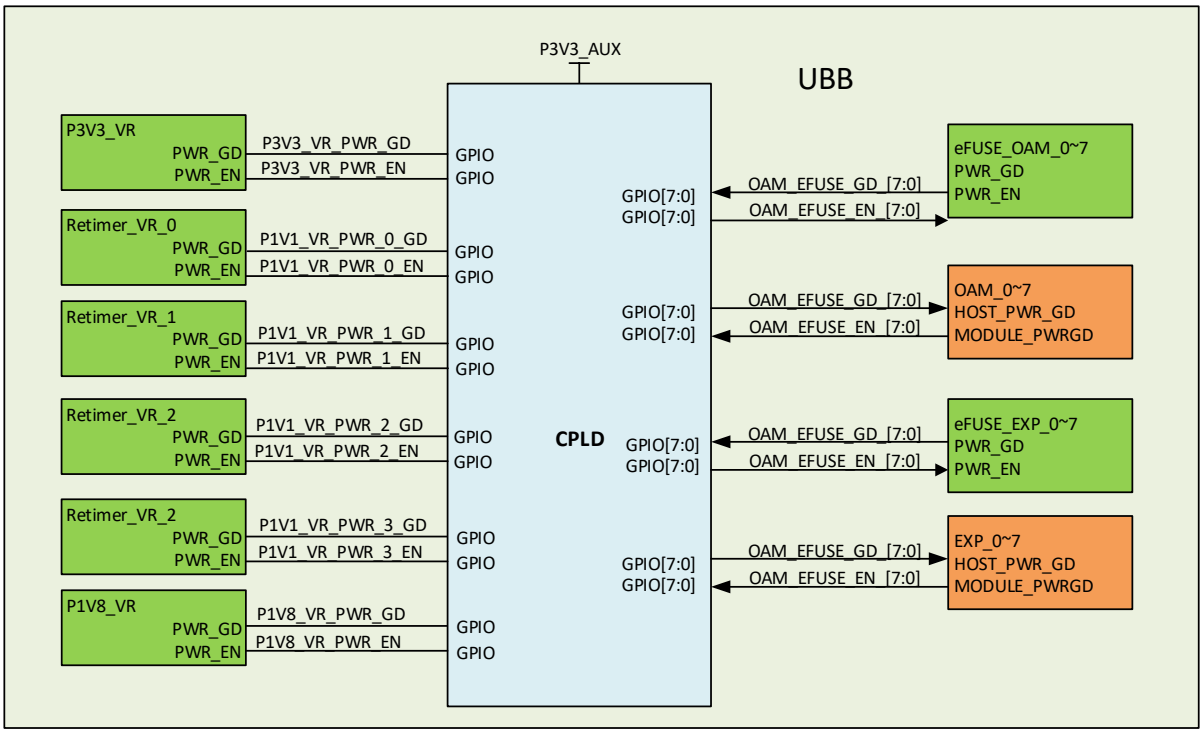


Figure 14 Power Control Block Diagram

7.1.6. Strap pins

7.1.6.1. OAM Module ID

Figure 15 shows the OAM MODULE_ID[4:0] strapping for physical orientation of 8x OAM.

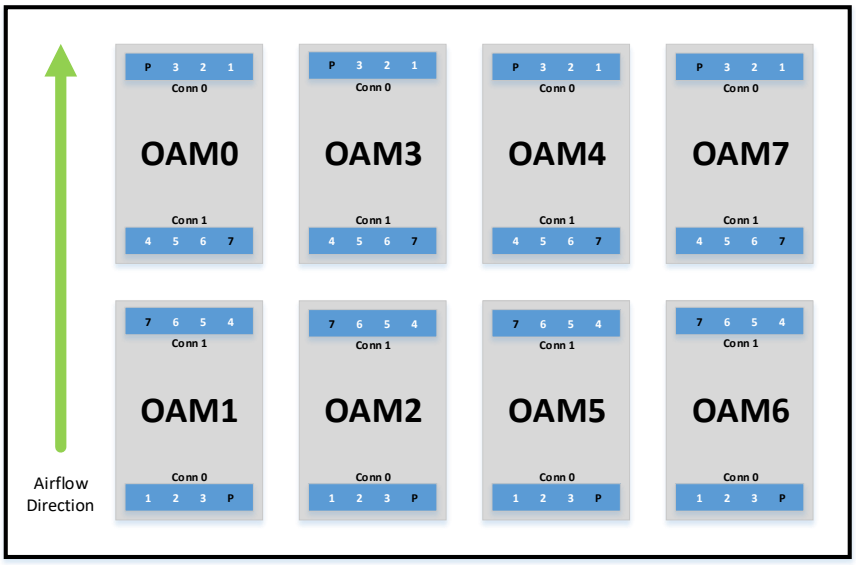


Figure 15 Required OAM MODULE_ID[4:0] assignments for UBB with 8x OAM

Figure 16 shows the OAM MODULE_ID[4:0] strapping for physical orientation of 4x OAM.

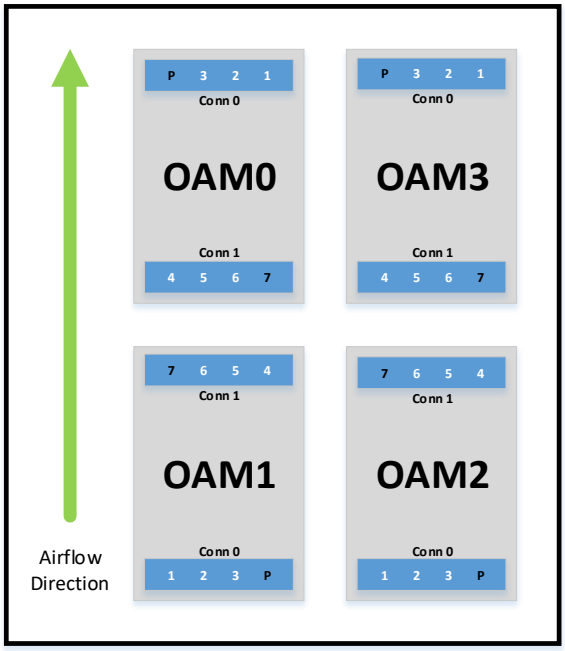


Figure 16 OAM Module_ID[4:0] assignments for UBB with 4x OAM

OAM MODULE_ID can be used as the I2C address strap pins if needed.

Table 7 OAM MODULE_ID

OAM	OAM Module ID
OAM0	00000
OAM1	00001
OAM2	00010
OAM3	00011
OAM4	00100
OAM5	00101
OAM6	00110
OAM7	00111

7.1.6.2. EXP Module ID

EXP MODULE_ID can be used as the I2C address strap pins if needed.

Table 8 EXP MODULE_ID

EXP	EXP Module ID
EXP0	000
EXP1	001
EXP2	010
EXP3	011
EXP4	100
EXP5	101
EXP6	110
EXP7	111

7.1.6.3. Link_Config[4:0]

The five link configuration strapping bits are pulled up on OAM. These bits are strapped to the ground on the baseboard to select logic 0 or left floating to select logic 1. Some OAMs use these LINK_CONFIG[4:0] strapping bits to determine the interconnect topology for the links between modules and determine the protocol of the "P" Link. Refer to Chapter 7.2 for details.

7.1.6.4. PE_BIF[1:0]

x16 Host Interface Bifurcation Configuration. This module output informs the host if it needs to bifurcate the PCIe interface to the module.

00 = one x16 PCIe host interface
01 = bifurcation into two x8 PCIe host interfaces
10 = bifurcation into four x4 PCIe host interfaces
11 = reserved

7.1.7. Debug interface

There are two OAM debug interfaces on UBB, one is JTAG, and the other is the UART interface. UART supports both micro USB local access and BMC's remote debugging feature. BMC console can access all OAMs UART at the same time.

There is also one debug header on UBB to support OAM debug through external dongle.

Below are JTAG, UART, and debug header diagrams.

7.1.8. JTAG Interface

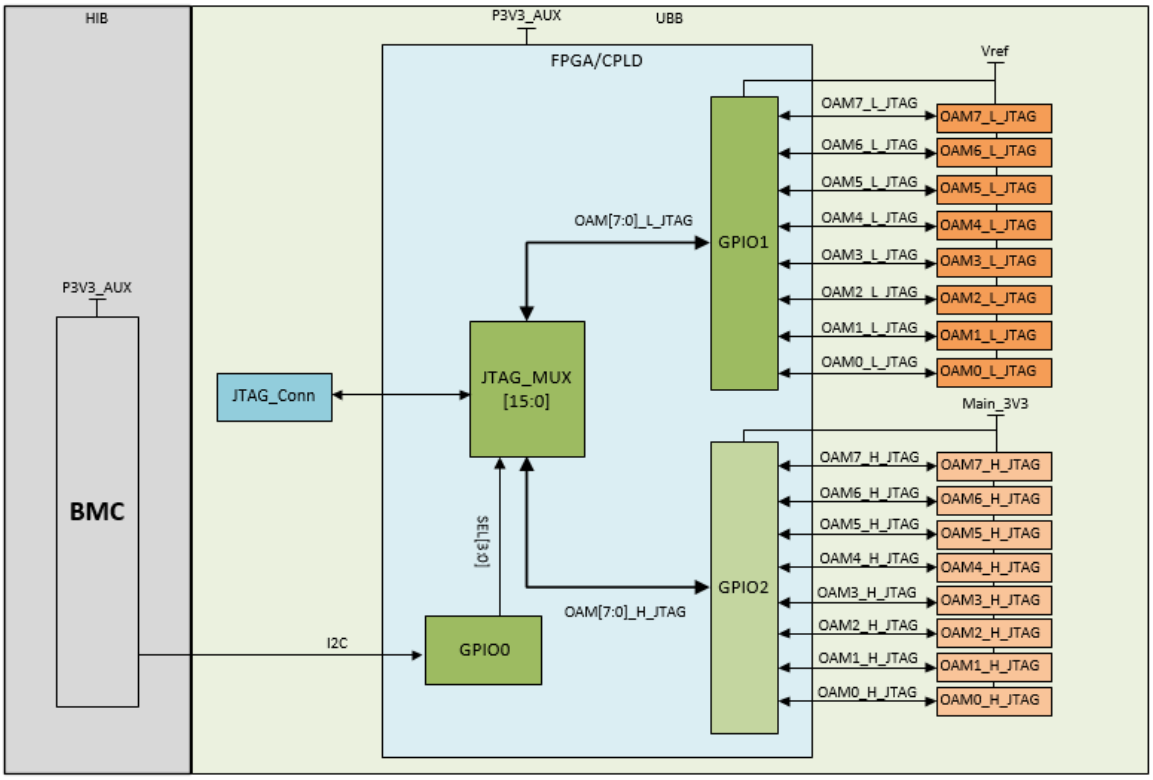


Figure 17 JTAG diagram

7.1.9. UART

OAM UART can be accessed by BMC or external Micro USB through USB Mux. The USB Hub diagram is shown below. Micro USB takes priority when plugged in and BMC will be notified through USB_Mux_Sel signal when a micro USB connector is plugged in.

BMC console can access all OAMs UART at the same time.

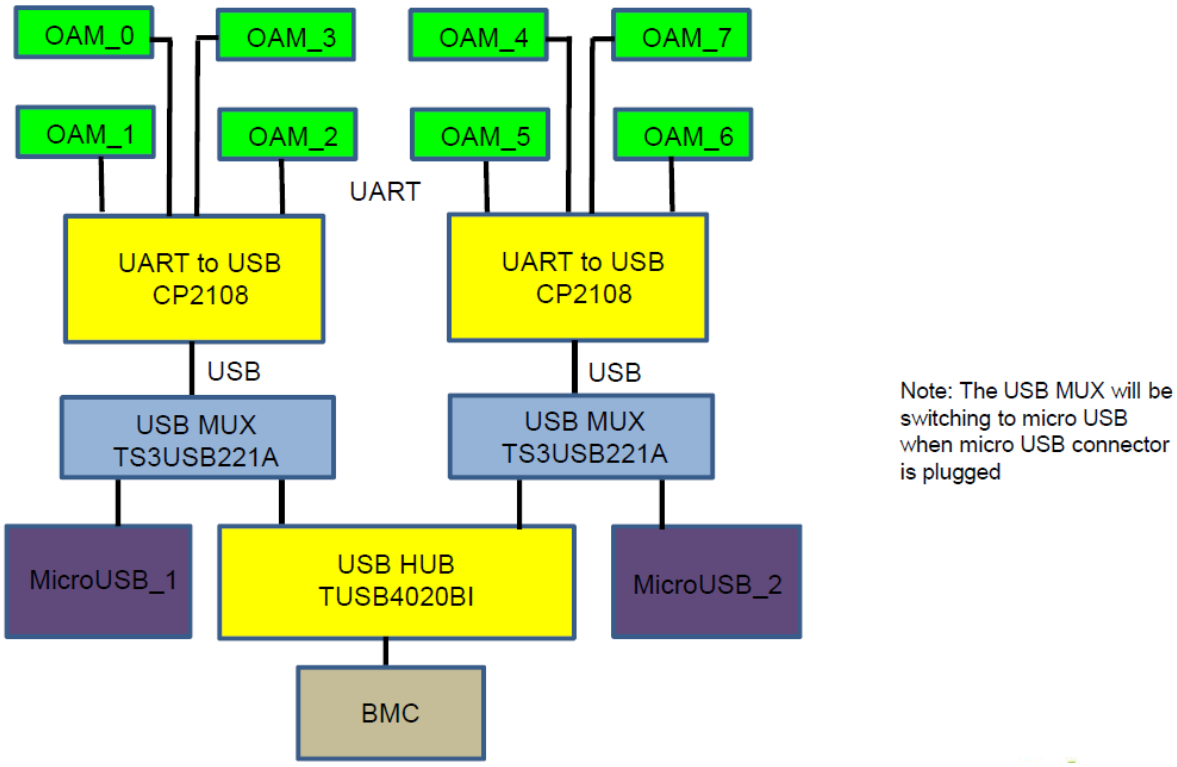


Figure 18 UART Diagram

7.1.10. Debug Header

A debug header is combined with proprietary debug interfaces from different OAM vendors by using OAM test pins. The debug header is optional in UBB spec. The one used in the OAI UBB reference design is Molex 501190-4017 with pin definition below:

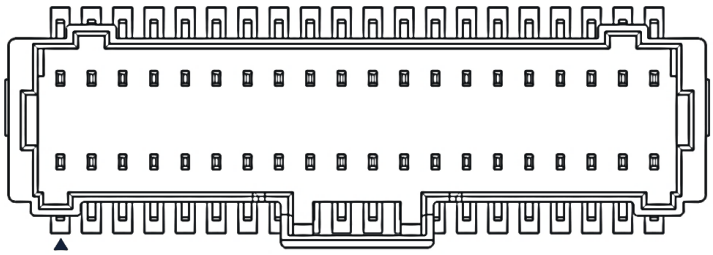


Figure 19 UBB reference board debug header

Table 9 UBB debug header pin definition

2	OAM_TEST_0	NC	1
4	OAM_TEST_1	NC	3
6	OAM_TEST_2	NC	5

8	OAM_TEST_3	NC	7
10	OAM_TEST_4	NC	9
12	OAM_TEST_5	NC	11
14	OAM_TEST_6	GND	13
16	OAM_TEST_7	GND	15
18	OAM_TEST_8	GND	17
20	OAM_TEST_9	GND	19
22	OAM_TEST_10	GND	21
24	OAM_TEST_11	JTAG_HOOK0	23
26	OAM_TEST_12	JTAG_HOOK6	25
28	OAM_TEST_13	JTAG_HOOK7	27
30	OAM_TEST_14	GND	29
32	GND	JTAG_TCK	31
34	NC	JTAG_TDO	33
36	VREF	JTAG_TRST	35
38	NC	JTAG_TDI	37
40	DEBUG_PRESENT_N	JTAG_TMS	39

7.1.11. UBB Power sequence

UBB board power sequence diagrams are shown below.

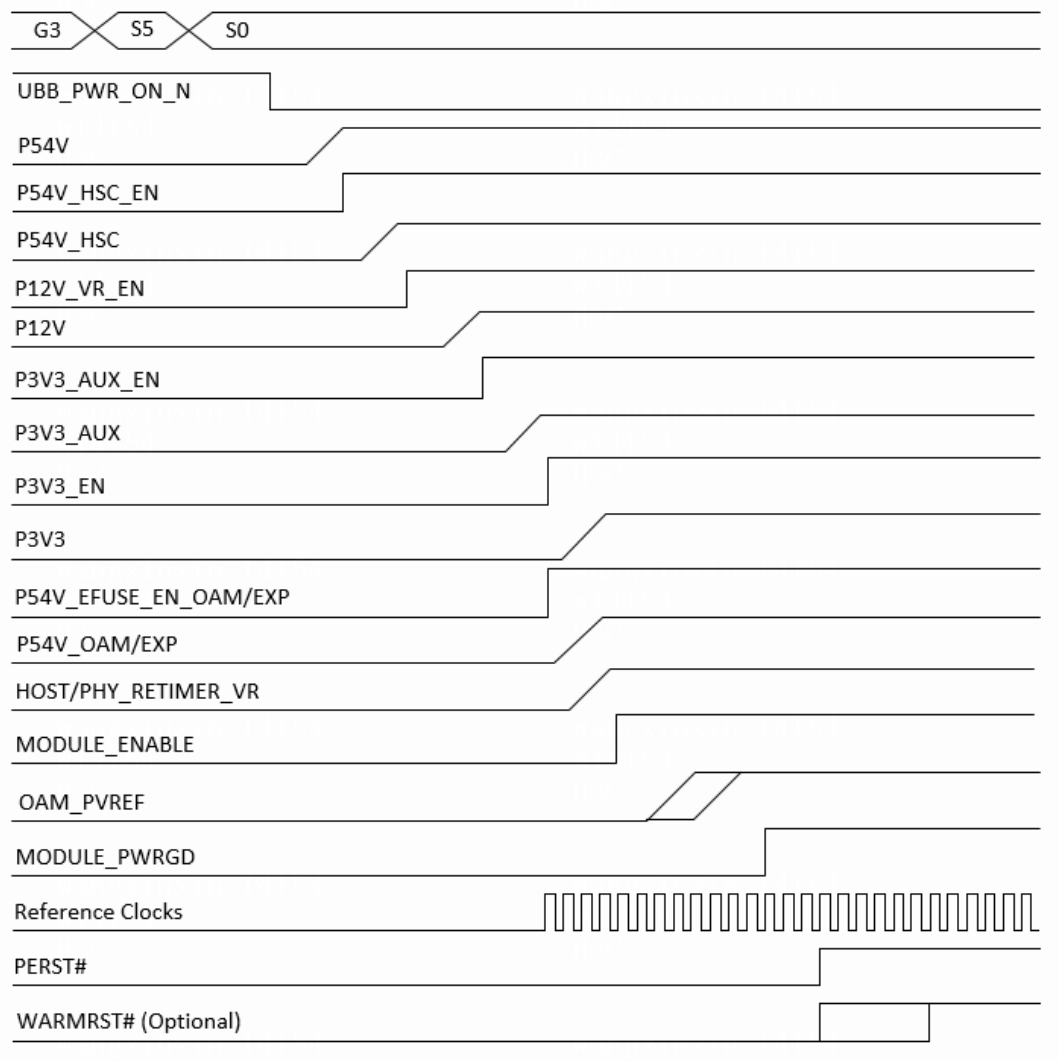


Figure 20 UBB Power-on sequence

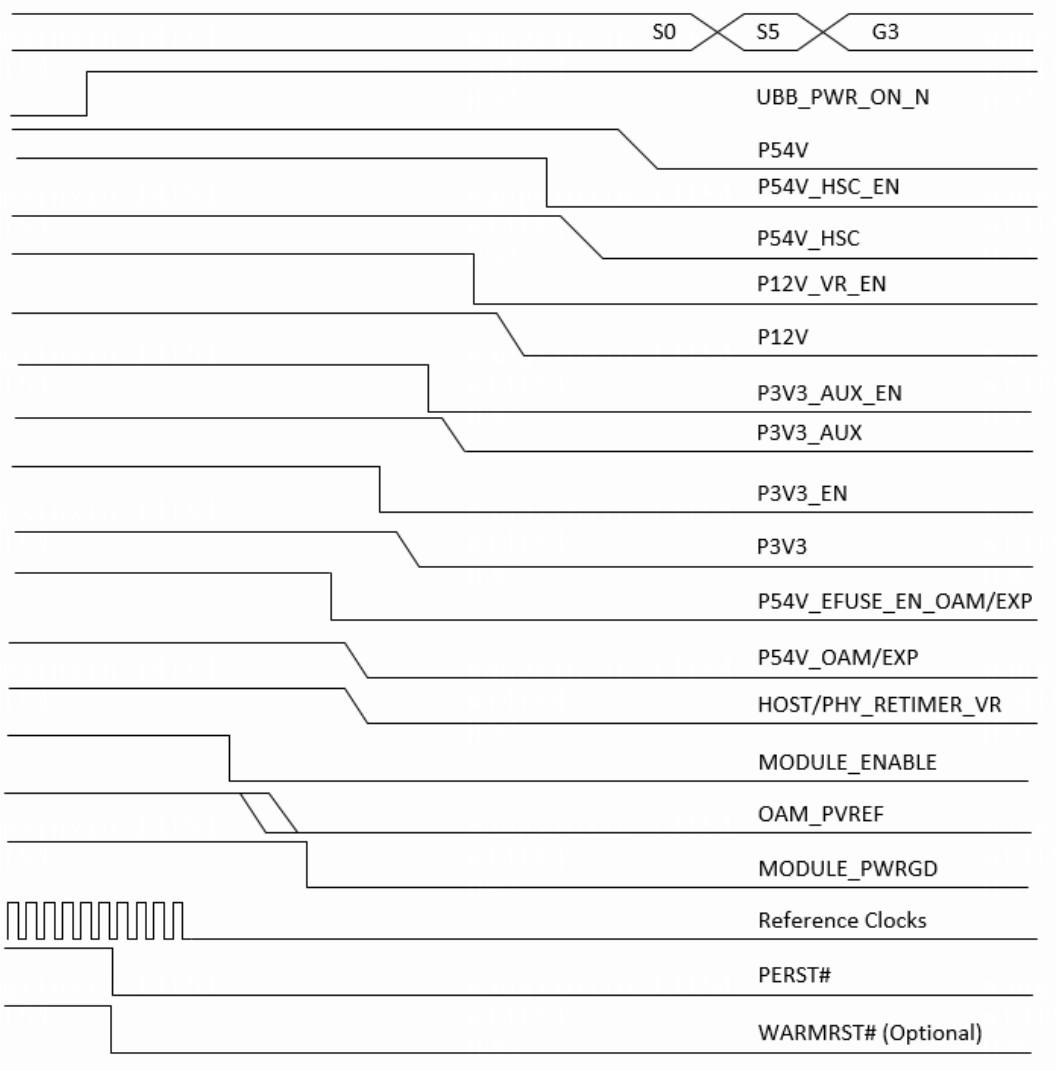


Figure 21 UBB Power-down sequence

Notes:

1. All voltages on the UBB must be within specification before MODULE_ENABLE is asserted.
2. HOST/PHY_RETIMER_VR depends on the system provider's design to be in the UBB design or not.
3. The MODULE_ENABLE is the UBB power good indication signal.
4. As the voltage planes on the UBB ramp up, the reference clocks from the UBB will begin to run.
5. After all the voltages on the module are within specification, the module asserts MODULE_PWRGD to the UBB.
6. At least 100ms after MODULE_PWRGD assertion, the UBB will de-assert the PCIe reset signal(PERST#) to the module.
7. The optional WARMRST# signal de-asserts simultaneously or later than the PERST# signal is de-asserted.

8. Using clock buffer enables the pin to control reference clock disable earlier than P3V3_EN.
9. Clock buffer enables pins to connect to CPLD.
10. After MODULE_ENABLE de-asserted, if Module_PWRGD doesn't de-asserted in 100ms, shut down all power rails.
11. UBB_PWR_ON_N is monitored by CPLD on HIB

7.1.12. PHY Retimer Management

By default, PHY retimers on EXP cards are managed by BMC on HIB. BMC is responsible for initializing retimers, loading firmware as well as performing runtime controls. The FPGA on UBB will convert BMC interface (e.g., I2C or PCIe) to the host interfaces supported by PHY retimers, typically SPI or MDC/MDIO. For backwards compatibility, UBB may also support the option to manage PHY retimers by individual OAMs, as shown in Figure 12.

When SPI bus is used for PHY retimer management, it is recommended to run the bus at 10MHz clock speed to benefit from high-speed device access and quick firmware download. It is further recommended to have two SPI buses, one for every four EXP slots. For each SPI bus, FPGA is the SPI master, and retimers are the SPI slaves. Separate clock trace per EXP running at 10MHz has proven to provide satisfactory SI performance.

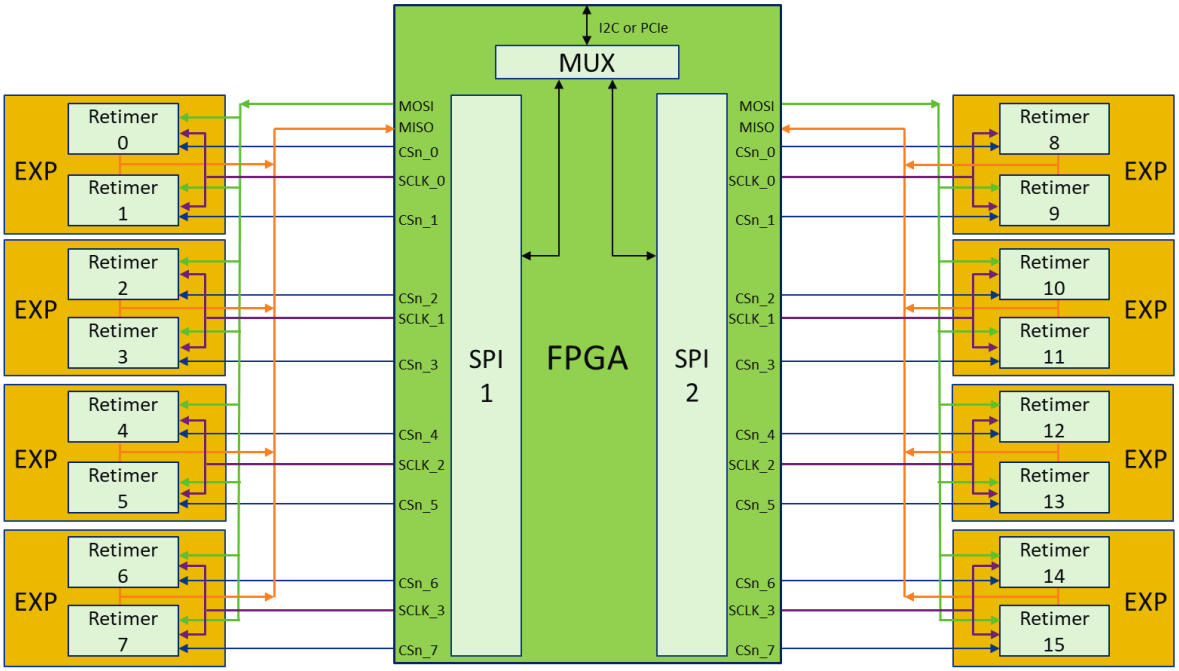


Figure 22 SPI for PHY Retimer (x16 links) Management

When MDC/MDIO is used for PHY retimer management, it is recommended to have a separate MDC/MDIO bus for each EXP slot. As shown in Figure 23, all four PHY retimers with x8 links on the same EXP card will share a single bus.

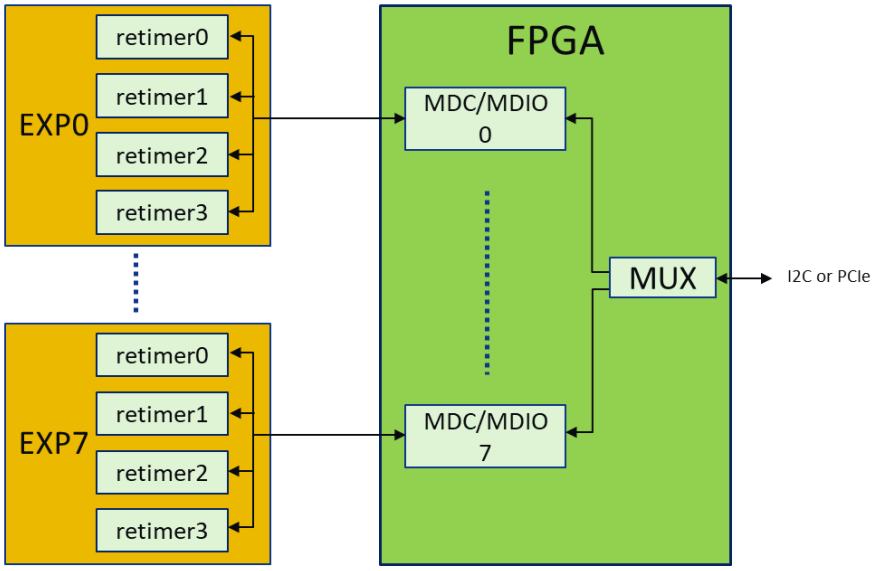


Figure 23 MDC/MDIO for PHY Retimer (x8 links) Management

8. UBB Connectors

UBB has one 6x8 high-density connectors and seven 4x8 high-density connectors, 16 OAM MMPro connectors, 8/16 EXP ExaMax and eight Gen-Z 2C connectors, eight mechanical guide pins and eight mechanical Wrench Fastener for EXP, four mechanical guide pins for UBB, six 54V power connectors, (can be repurposed for 54V power delivery, see 6.2.1.4), two micro-USB UART ports, and four RoT connector(optional). Details are in the table below.

Table 10 UBB connector list

Board	Vendor	Vendor PN	Description	Q'ty	Designation	R/V	Solder Type
UBB	Molex	218910-1115/218916-1115	OAM Connector 2.5mm/5.5mm	16	OAM Module	VT	SMT
	Southco	P7-99-1260	EXP Ejector Fastener	8	EXP Module	VT	/
	ACES	59493-0050D-CH1	Micro USB Connector	2	UBB	RA	SMT
	Amphenol	10061289-001LF(2x3)	AirMax 54V Input 2x3	2	54V Power/GND	RA	Press-Fit
	Amphenol	10028917-001LF(2x2)	AirMax 54V Input 2x2	2	54V Power/GND	RA	Press-Fit
	Amphenol	10136689-003LF	PwrMax 54V Input	2	54V Power/GND	RA	Press-Fit
	Amphenol	10131762-301LF	EXAMAX PCIe Connector 6x8 RAR (PCIe Gen5)	1	PCIe Gen5	RA	Press-Fit
	Amphenol	10137002-101LF	EXAMAX PCIe Connector 4x8 RAR (PCIe Gen5)	7	PCIe Gen5	RA	Press-Fit
	Amphenol	10037909-101LF(Single Pin)	Guide Pin Receptacle	4	Guide	RA	Press-Fit + Screw
	Amphenol	10167063-101LF	EXAMAX2 EXP Connector 4X16 VT Header	8/16	EXP Module 112G PAM4 signal	VT	Press-Fit
	Amphenol	ME1008410121011	Gen-Z 2C 2.36mm EXP Connector VT	8	EXP Module Sideband & power	VT	SMT
	Amphenol	10158690-109LF	EXP Guide Pin on UBB board	8	EXP Module Guide	VT	Press-Fit + Screw
	Amphenol	61082-04XXXXXX	RoT Connector	4	RoT	VT	SMT

8.1. UBB Connector pin list

This chapter describes connectors including Host Interface, 54V power, EXP, debug header.

8.1.1. EXP module connector pin list

EXP Module pinlist and pin map please refer to *OAI-EXP_Pinlist_Pinmap_r2.0_v1.0.xlsx*.

8.1.2. 54V power connector pin list

Base on temperature rise under 30˚C, 25Amp per contact (POS).

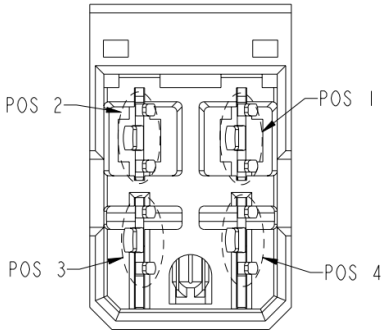
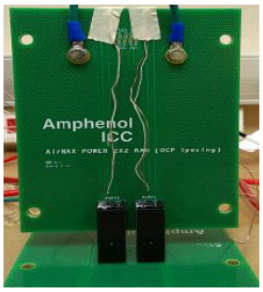
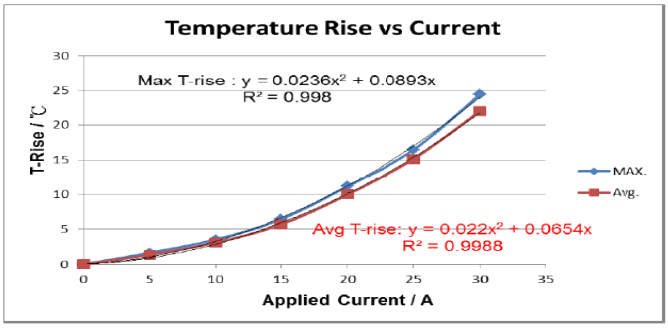


Figure 24 54V power connector

54V power derating spec

Applied Current/A	5	10	15	20	25	30	32
Max T-rise/℃	1.63	3.53	6.46	11.17	16.46	24.38	29.31
Avg. of Max T-rise/ ℃ of each sample/℃	1.35	3.10	5.69	9.99	15.15	22.00	27.08





- The thermal test for the vertical connector, the Max T-rise, is around 12°C, 20A.

P54V_0 Pin Definition:

Table 11 P54V_0 Pin Definition

POS 1 & 2	54V_1	54V_0
POS 3 & 4	GND	GND

P54V_1 Pin Definition:

Table 12 P54V_1 Pin Definition

POS 1 & 2	54V_2	54V_3
POS 3 & 4	GND	GND

P54V_2 Pin Definition:

Table 13 P54V_2 Pin Definition

POS 1 & 2	54V_4	54V_5
POS 3 & 4	GND	GND

P54V_3 Pin Definition:

Table 14 P54V_3 Pin Definition

POS 1 & 2	54V_7	54V_6
POS 3 & 4	GND	GND

8.1.3. Host Interface Connector (HIF) pin list

This chapter describes the Host Interface connector (HIF). There are 8 connectors. The signal direction of HIF0~7 in the table below is based on the UBB side. Detailed pin map is in UBB spec package available on OAI Wiki, please refer to *OAI-UBB_Pinlist_r2.0_v1.0.xlsx.*

8.1.4. OAM Debug connector pin list

Molex 501190-4017 is selected, total pin count is 40pin

Current – Maximum per contact is 1A

Voltage – Maximum is 50V AC (RMS)/DC

All signals direction are based on the UBB side

Table 15 OAM Debug connector pin list

Signal	UBB Direction POV	Description	Voltage	Required or Optional	Pin Assignment	Total Single Pins
GND		GND		Required	13,15,17,19,21,29,32	7
JTAG_TMS	Input	Low Voltage ASIC/GPU JTAG Test Mode Select	Vref(OAM)	Required	39	1
JTAG_TDI	Input	JTAG master data output	Vref(OAM)	Required	37	1
JTAG_TCK	Input	ARM JTAG clock output	Vref(OAM)	Required	31	1
JTAG_TDO	Output	JTAG master data input	Vref(OAM)	Required	33	1
JTAG_TRST	Input	JTAG master reset output	Vref(OAM)	Required	35	1

DEBUG_PRESENT_N	Input	Present of debug connector	3.3V	Required	40	1
P1V8 (*)	Power input	Power for debug connector	Vref(OAM)	Required	36	1
Hook[0]	Output	Debug signals	3.3V	Required	23	1
Hook[6,7]	Output	Debug signals	Vref(OAM)	Required	25,27	2
OAM_TEST [0-14]	Input/ Output	Debug signals	Vref(OAM)	Required	2,4,6,8,10,12,14,16,18,20,22,24,26,28,30	15
NC					1,3,5,7,9,11,34,38	8

***Note:** This power pin is for debugging connectors. ODM design should base on its debug tool voltage requirement.

8.2. PCB Stack-Up

This section describes the OAI UBB reference board stack-up and requirements. The OAI UBB reference board (based on 11-port FC/Retimer Topology) uses 30 layers PCB stack-up with 800G Ultra-low loss material. To support high TDP OAM (54V/48V up to 1000W) and high-speed interconnect(up to 112Gbps PAM4), the PCB stack-up adheres to the following requirements:

- PCB with up to four 2oz layers to meet the required copper density
- 85 & 90 Ohms differential traces in internal signal layers as needed.
- 45 & 50 Ohms or single-ended traces as required (Depending on the chip vendor's design guide)
- PCB material depends on the maximum trace length of topology design and meets the vendor’s channel loss criteria.
- Back Drilling for signals on Layer 5, 7, 9, 11, 13, 18, 20, 22, 24, and 26 to remove stubs from SerDes and PCIe Gen5/6 via transitions. Limit back drilling to 1mm from the top layer to help press-fit contact.

UBB reference board uses below stack up. Each vendor must fine-tune the width/spacing design based on the material target and impedance control table below.

Table 16 UBB reference Stack-Up

Layer	Plane Description		Copper (OZ)	Thickness (mil)
		Solder mask		0.5
L1	Top	Signal/PWR	0.5oz + plating	1.9
		PrePreg		3.2
L2	GND1	Ground	1.0	1.2
		Core (1/1)		4
L3	VCC1	Power	2.0	2.4
		PrePreg		5
L4	GND2	Ground	1.0	1.2
		Core (1/1)		4
L5	IN1	Signal/PWR	0.5	0.6
		PrePreg		5
L6	GND3	Ground	0.5	0.6
		Core (1/1)		4
L7	IN2	Signal/PWR	0.5	0.6
		PrePreg		5
L8	GND4	Ground	0.5	0.6
		Core (1/1)		4
L9	IN3	Signal/PWR	0.5	0.6
		PrePreg		5
L10	GND5	Ground	0.5	0.6
		Core (1/2)		4
L11	IN4	Signal/PWR	0.5	0.6
		PrePreg		5
L12	GND6	Ground	0.5	0.6
		Core (1/2)		4
L13	IN5	Signal/PWR	0.5	0.6

		PrePreg		5
L14	GND7	Ground	1.0	1.2
		Core (1/1)		4
L15	VCC2	Power	2.0	2.4
		PrePreg		5
L16	VCC3	Power	2.0	2.4
		Core (1/1)		4
L17	GND8	Ground	1.0	1.2
		PrePreg		5
L18	IN6	Signal/PWR	0.5	0.6
		Core (1/1)		4
L19	GND9	Ground	0.5	0.6
		PrePreg		5
L20	IN7	Signal/PWR	0.5	0.6
		Core (1/1)		4
L21	GND10	Ground	0.5	0.6
		PrePreg		5
L22	IN8	Signal/PWR	0.5	0.6
		Core (1/1)		4
L23	GND11	Ground	0.5	0.6
		PrePreg		5
L24	IN9	Signal/PWR	0.5	0.6
		Core (1/1)		4
L25	GND12	Ground	0.5	0.6
		PrePreg		5
L26	IN10	Signal/PWR	0.5	0.6
		Core (1/1)		4
L27	GND13	Ground	1.0	1.2

		PrePreg		5
L28	VCC4	Power	2.0	2.4
		Core (1/1)		4
L29	GND14	Ground	1.0	1.2
		PrePreg		3.2
L30	BOT	Signal/PWR	0.5oz + plating	1.9
		Solder Mask		0.5
		Total		160mil (with +/- 10% tolerance)

Table 17 UBB Impedance control

Trace Width (mil)	Air Gap Spacing (mil)	Impedance Type	Layer	Impedance Target (ohm)	Tolerance (+/- %)
7.2		Single-Ended	1,30	45	10%
6.0		Single-Ended	1,30	50	10%
7	6	Differential	1,30	85	10%
6.5	6.5	Differential	1,30	90	10%
6.1		Single-Ended	5,7,9,11,13,18,20,22,24,26	45	10%
5		Single-Ended	5,7,9,11,13,18,20,22,24,26	50	10%
6.3	6.7	Differential	5,7,9,11,13,18,20,22,24,26	85	10%
5.8	7.2	Differential	5,7,9,11,13,18,20,22,24,26	90	10%

8.3. UBB CPLD/FPGA

8.3.1. Fan-out signal to 8 OAMs

CPLD receives PERST and PWRBRK signals from the host interface board, and then fan out to the 8 OAMs individually, see Table 18 and Figure 13.

Table 18 CPLD/FPGA Fan-out to OAMs

Module	Input	Fan Out
OAM_PERST	HOST_PERST_N	OAM[7:0]_PERST_N
OAM_Power_Break	OAM_PWRBRK_N	OAM[7:0]_PWRBRK_N

8.3.2. OAM Test Pins

OAM test pins are connected to CPLD/FPGA and reroute to debug header for debugging purposes. Below is a pin list of these 14 test pins.

Table 19 OAM test pins definition

Signal	Module Direction POV	Description	Voltage	Required or Optional
OAM_TEST0	Output	Test pin	V_{ref}	Optional
OAM_TEST1	Output	Test pin	V_{ref}	Optional
OAM_TEST2	Output	Test pin	V_{ref}	Optional
OAM_TEST3	Output	Test pin	V_{ref}	Optional
OAM_TEST4	Output	Test pin	V_{ref}	Optional
OAM_TEST5	Input/Output	Test pin	V_{ref}	Optional
OAM_TEST6	Input/Output	Test pin	V_{ref}	Optional
OAM_TEST7	Input	Test pin	V_{ref}	Optional
OAM_TEST8	Output	Test pin	V_{ref}	Optional
OAM_TEST9	Output	Test pin	V_{ref}	Optional
OAM_TEST10	Output	Test pin	V_{ref}	Optional
OAM_TEST11	Input	Test pin	V_{ref}	Optional
OAM_TEST12	Output	Test pin	V_{ref}	Optional
OAM_TEST13	Output	Test pin	V_{ref}	Optional
OAM_TEST14	Output	Test pin	V_{ref}	Optional

8.3.3. OAM Vref based IO Pin

The table below shows OAM Vref based miscellaneous signal list. The level shift devices and open-drain output are for reference only.

All miscellaneous signal power sources have to connect to their OAM Vref output per the block diagram illustrated. For open-drain I/O connected to the OAM Vref signal, the pull-up resistors' power is connected from its OAM Vref. For a level shift device with two power sources, the high voltage power

source comes from UBB power, and the low voltage power source comes from its OAM Vref power. The level shift component (ex: NXP NTS0104) must act as a power isolation device between OAM Vref and CPLD/FPGA, High-Density connector, EXP.

Table 20 OAM Vref Signal usage

OAM Miscellaneous Vref signals				
Signal	Direction	I/O Type	UBB Connection Device	Connector
PVREF	Power Output	Power	OAM Output (1.5V ~ 3.3V)	Conn0
WARMRST#	Input		CPLD GPIO.OD w/ PU	Conn0
MODULE_ID	Input	Internal 47K PU	0: 100ohm 1: Floating	Conn0
LINK_CONFIG[4:0]	Input	Internal 47K PU	0: 100ohm 1: Floating	Conn1
PE_BIF[1:0]	Output	0: 1K ohm PD 1: 10K ohm PU	100K ohm PU	Conn1
PLINK_CAP	Output	0: 1K ohm PD 1: 10K ohm PU	100K ohm PU	Conn1
I2C_D	I/O	I/OD	PCA9617A w/PU	Conn0
I2C_CLK	Output	OD	PCA9617A w/PU	Conn0
JTAG0_TRST	Input		CPLD GPIO.OD w/PU	Conn0
JTAG0_TMS	Input		CPLD GPIO.OD w/PU	Conn0
JTAG0_TCK	Input		CPLD GPIO.OD w/PU	Conn0
JTAG0_TDO	Output	Push-Pull	CPLD GPIO Input	Conn0
JTAG0_TDI	Input		CPLD GPIO.OD w/PU	Conn0
DEBUG_PORT_PRSNT#	Input		CPLD GPIO.OD	Conn1
TEST[0:4]	Input		CPLD GPIO.OD	Conn0
TEST[5:9]	I/O	Push-Pull (I/O)	CPLD GPIO.OD w/PU or level shift device	Conn0
TEST[10:14]	I/O	Push-Pull (I/O)	CPLD GPIO.OD w/PU or level shift device	Conn1
TEST_MODE#	Input		DIP_SW w/PU	Conn0

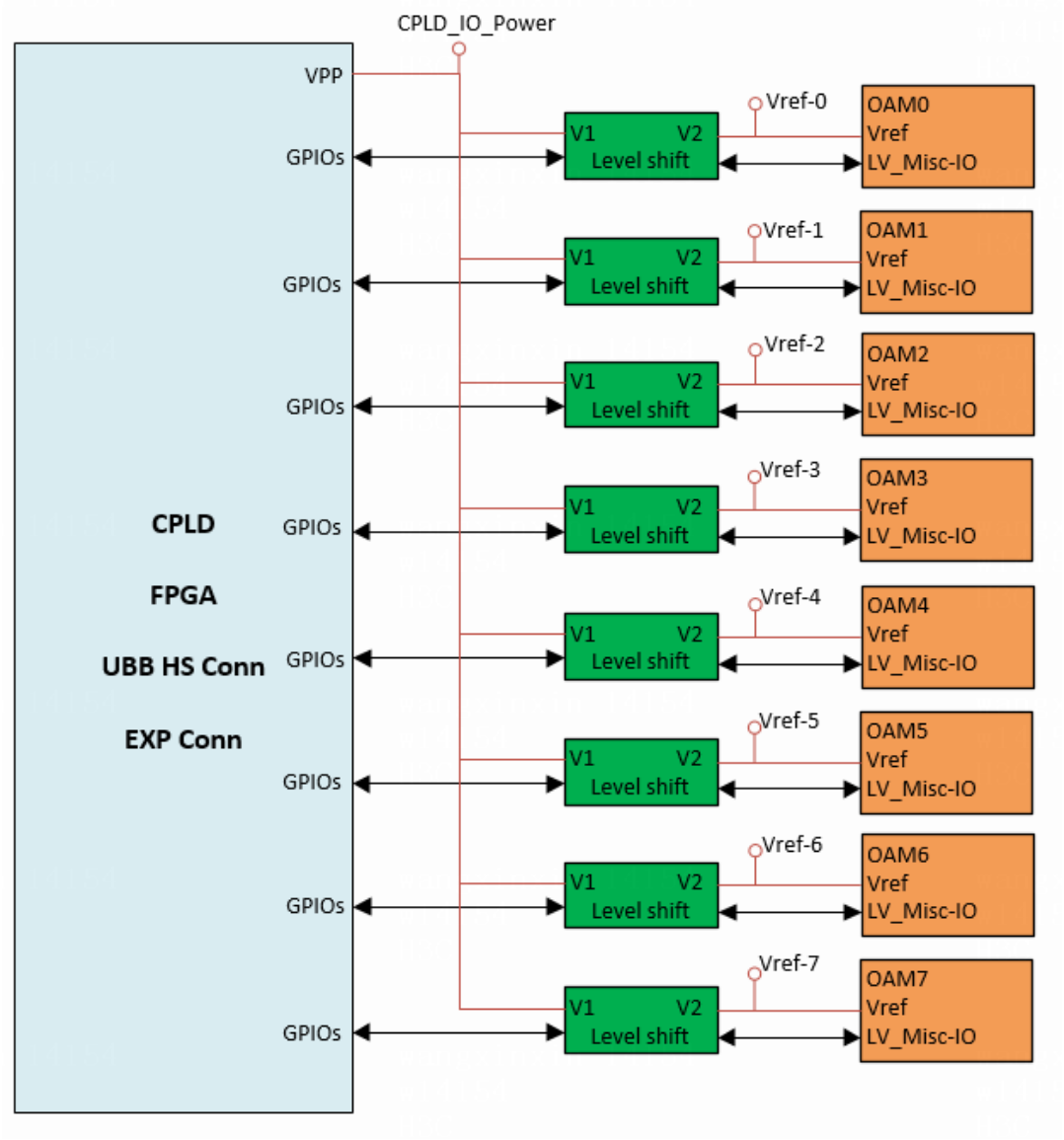


Figure 25 Vref Signal Block Diagram

The table below shows the CPLD/FPGA Vccio power source and input/output pin power level from Lattice MachXO2 for reference. The Vccio power source must be connected from UBB VR power output, not from the OAM Vref output. The CPLD Vccio 1.5V supports OAM Inputs I/O voltage wider range (1.2V ~ 3.3V). The Outputs I/O should be set to open-drain for a broader range Vref.

Table 21 Mixed Voltage Support for LVCMOS and LVTTL I/O Types (copied from Lattice MachXO2 datasheet)

	Inputs					Outputs				
V_{CCIO}	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	YES	YES[6]				YES				
1.5 V	YES[1]	YES	YES[6]	YES[6]	YES[6]		YES			
1.8 V	YES[1]	YES[5]	YES	YES[6]	YES[6]			YES		
2.5 V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES	YES[6]				YES	
3.3 V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES[4, 5, 7]	YES					YES

8.4. Host Retimer

System design decides whether host retimers need for their UBB design. OAI reference UBBs implemented eight of the 16x lane retimer device (ex: PCIe G5, 32GT/s) to near the ExaMax connector. Each 16x lane retimer supports a standard clock between HIB and retimer and retimer to OAM (refer to 6.1.1). The upstream of the retimer lane is the HIB lane root port. The retimer topology is shown in figure below.

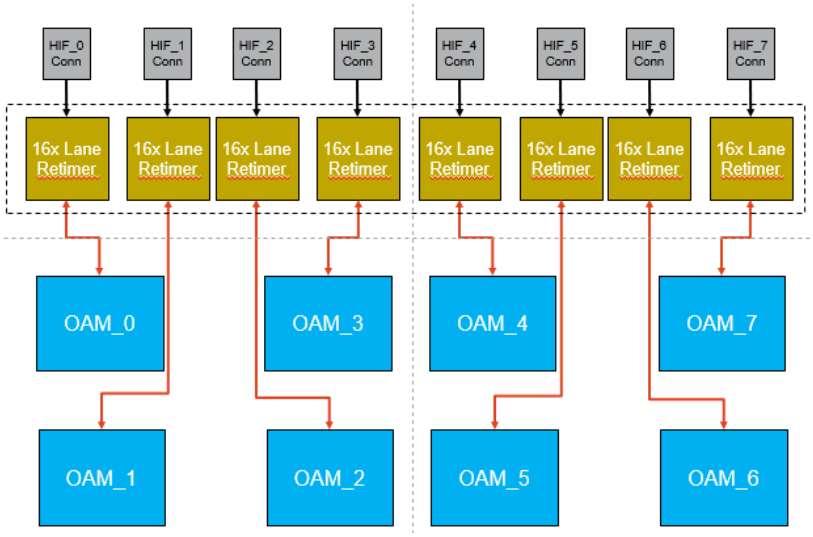


Figure 26 HIB Lane Retimer Topology

8.5. RoT Security Management Module

The UBB Security Management Module provides the following function. UBB Security Management Module physical specification is defined and recommend security chip for design reference.

- Secure boot provides a hardware-based root of trust (RoT).
- Easy-to-use, seamless authentication and encryption capabilities for connected applications.
- Robust hardware cryptography cypher suite.

The UBB Security Management Module block diagram is shown in figure below. There are two SPI topologies in the diagram for different applications of SPI ROM image verification and real time SPI operation code monitoring (Optional). Different security level ROT chip can be selected based on security level design requirement.

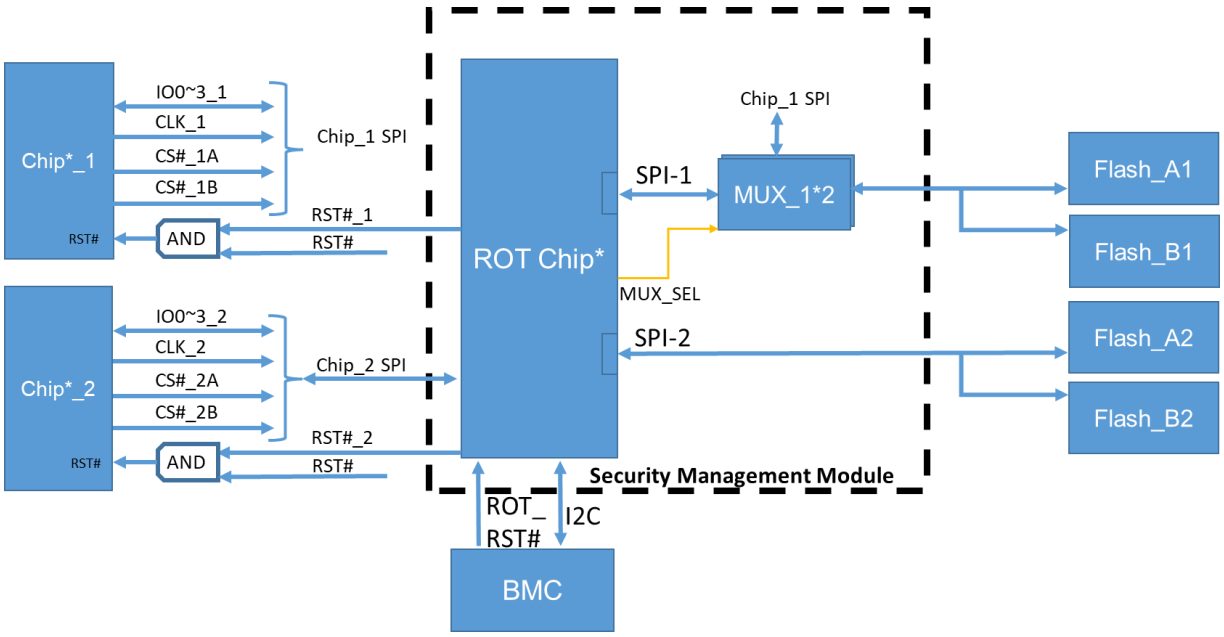


Figure 27 Security Management Module Block Diagram

Chip*: BMC and PCIe Switch…etc.

RoT Chip*: The Chip for SPI ROM image compares and monitor SPI interface (Optional).

Security Management Module pin list in table 22, the module to UBB connector is 40 pins board to board connector. In the Module side connector part number is Amphenol 61083-044602LF, and the connector supported maximum 0.8A/pin. In the UBB side connector part number is Amphenol 61082. Based on different height design between UBB and Security Management Module, it can be selected from different stack heights (8mm, 12mm, 16mm & 20mm) in Amphenol 61082.

Table 22 Security Management Module Pin List

Pin1	Pin2
P3V3	P3V3
Reserve	Reserve
GND	GND
IO0_1	IO0_1_Flash
IO1_1	IO1_1_Flash
IO2_1	IO2_1_Flash
IO3_1	IO3_1_Flash
CLK_1	CLK_1_Flash

CS#_1A	CS#_1A_Flash
CS#_1B	CS#_1B_Flash
RST#_1	ROT_RST#
IO0_2	IO0_2_Flash
IO1_2	IO1_2_Flash
IO2_2	IO2_2_Flash
IO3_2	IO3_2_Flash
CLK_2	CLK_2_Flash
CS#_2A	CS#_2A_Flash
CS#_2B	CS#_2B_Flash
RST#_2	Reserve
SDA	SCL
Pin39	**Pin40**

Security Management Module dimension and recommend placement is in the figure below. The module size is 25mm*30mm. The RoT chip recommended size is under 7mm*7mm, and SPI MUX (or buffer) recommend size is under 4.15mm*4.15mm. JTAG debug pin header is optional, can be pin header or test points.

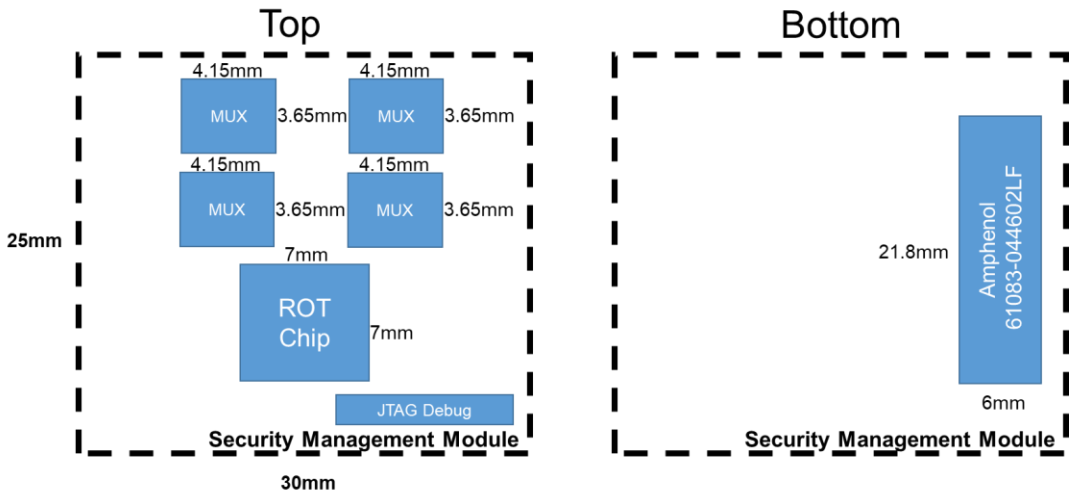


Figure 28 Security Management Module Dimension

Security Management Module ME Drawing and ISO View are in Figure 29 and 30. There is a M3 screw hole on the module that can be used to fix it to the UBB board.

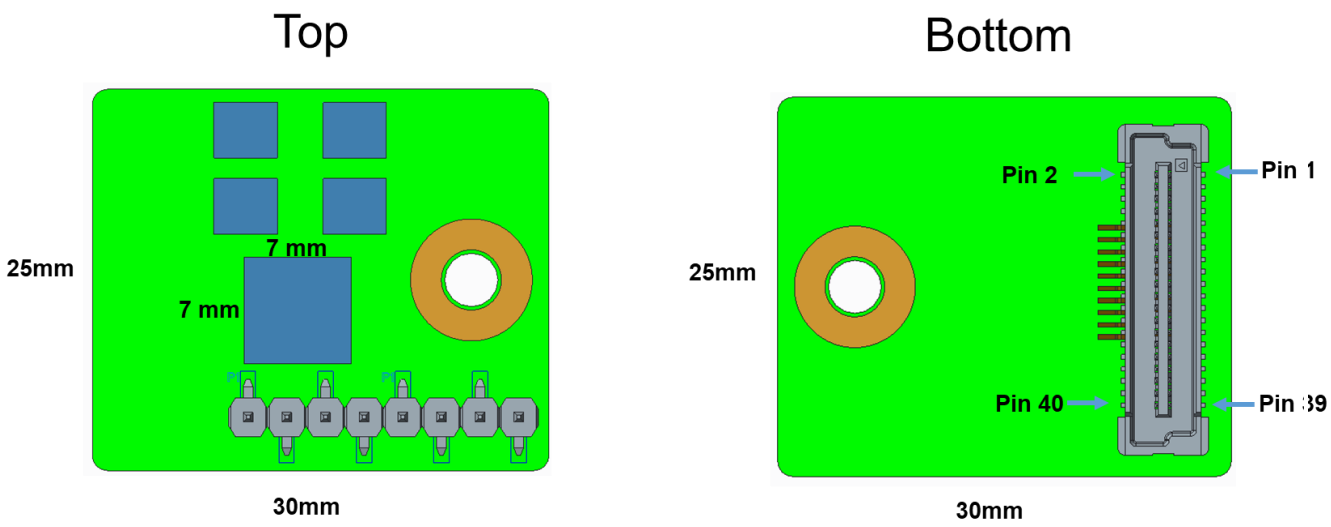


Figure 29 Security Management Module ME Drawing

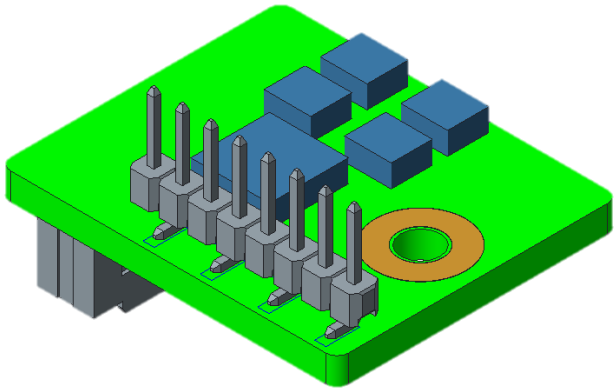


Figure 30 Security Management Module ISO View

Security Management Module reference chip list in table 23 with same package dimension (7*7 mm) and different security level RoT chip.

Table 23 Security Management Module Pin List

Vendor	Microchip	Microchip	STMicroelectronics	Nuvoton	Nuvoton
Part Number	CEC1736	CEC1712	STM32U575xx	M487SIDAE	M2351SIAAE
Package	84pin WFBGA	84pin WFBGA	UFBGA169	LQFP64	LQFP64

Voltage	1.8V and 3.3V	1.8V and 3.3V	1.71V to 3.6V	1.8V and 3.3V	1.8V and 3.3V
Processor	ARM Cortex-M4F	ARM Cortex-M4	ARM Cortex-M33	ARM Cortex-M4	ARM Cortex-M23
Clock	96MHz	48MHz	50MHz	192MHZ	64MHZ
SPI	2*Quad SPI	2*Quad SPI	Dual OCTOSPI	1*Quad SPI、4*SPI	1*Quad SPI、4*SPI
Security Level	NIST 800-193	NIST 800-193	NIST SP800-90B	AES(NIST 800-38A) ECC(NIST P192~521 、B163~571 、K163~571)	AES(NIST 800-38A) ECC(NIST P192~521 、B163~571 、K163~571)

9. Interconnect Topology

Universal baseboard supports 8 OAMs and can support different topologies described in OAM Base Specification section 9. This section describes two references interconnect topologies used in UBB reference boards.

9.1. OAM Module ID

There are 5 module ID pins defined in the OAM specification. UBB sets these pins based on the Table below.

Table 24 UBB OAM module IDs

OAM	OAM Module ID
OAM0	00000
OAM1	00001
OAM2	00010
OAM3	00011
OAM4	00100
OAM5	00101
OAM6	00110
OAM7	00111

9.2. LINK_CONFIG ID

Link_Config ID pins are defined in OAI-OAM Base Specification. The 5 link configuration strapping bits are pulled up on modules. These bits are strapped to the ground on the UBB to select logic 0 or left floating on the baseboard to select logic 1. Some accelerators use these LINK_CONFIG[4:0] strapping bits to determine the interconnect topology for the links between modules and determine the protocol of the “P” Link. UBB should set the Link_Config ID based on the table defined in OAM Base Specification.

Table 25 LINK_CONFIG[4:0] Encoding Definitions

LINK_CONFIG[4:0]	Definition
00000	Reserved for OAM. Test use by OAM Vendor.
xxxx0 (except for 00000)	Indicates the “P” link is PCIe.
0001x	Combined FC/6-Port HCM Topology.
0010x	8-Ports HCM Topology.
0011x	11-port (7+4) FC/Retimer Topology.

0100x	8-port Switch-Based Topology.
0101x	Fully Connected Topology.
0110x – 1xxxx	RSVD
xxxx1 (except for 11111)	Indicates the “P” link is an alternate protocol other than PCIe.
11111	Indicates an alternate means for identifying the link interconnect topology and configuration is used.

*This table is referenced from OAM Base Specification, and Encodings are not listed in the figure below.

The following figure shows the OAM ID and Configure ID connection. OAM ID has its MODULE_ID[4:0] connection to identify its module ID number. The configure ID must connect to all OAM LINK_CONFIG[4:0] and BMC.

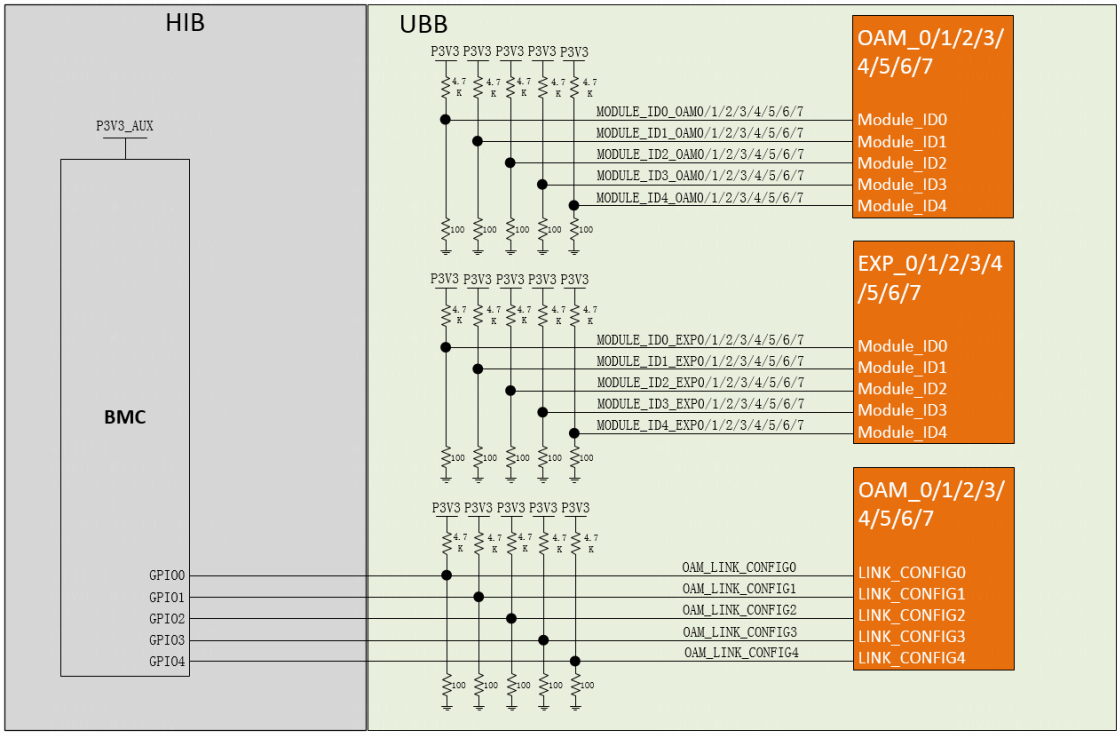


Figure 31 LINK_CONFIG ID

9.3. Fully Connected

If the module has 7 or more links, each can directly communicate with the other 7 modules. The topology is fully connected. Each link can be up to X16 in FC topology (no extra link or port for scale-out if it's X16 per the link here).

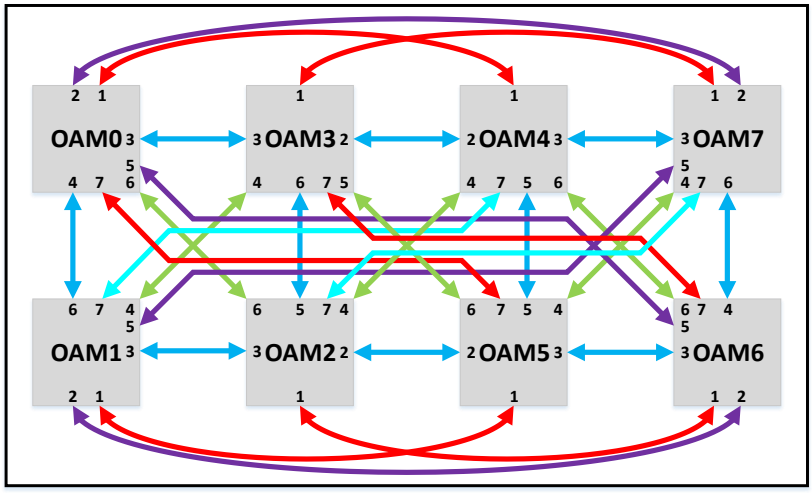


Figure 32 Fully Connected Topology

Here is the routing suggestion for 7X16 links fully connected topology:

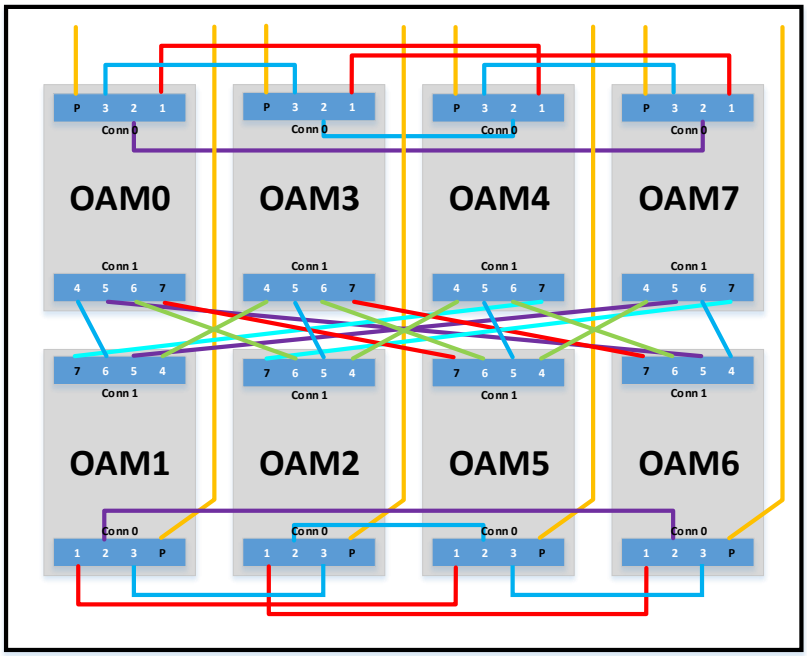


Figure 33 Routing Recommendation for Fully Connected Topology

9.4. Combined Fully Connected and 6-port Hybrid Cube Mesh Topology

For fully connect with expansion consideration, the UBB link is routed as x8(1st X8 of each port, 1L-7L), leaving 2nd x8 of each SerDes port for expansion or embedding other topology. Here is 8 port HCM UBB reference board 7X8 fully connected topology combined with 6X8 hybrid cube mesh topology (x8 FC + x8 6 port HCM):

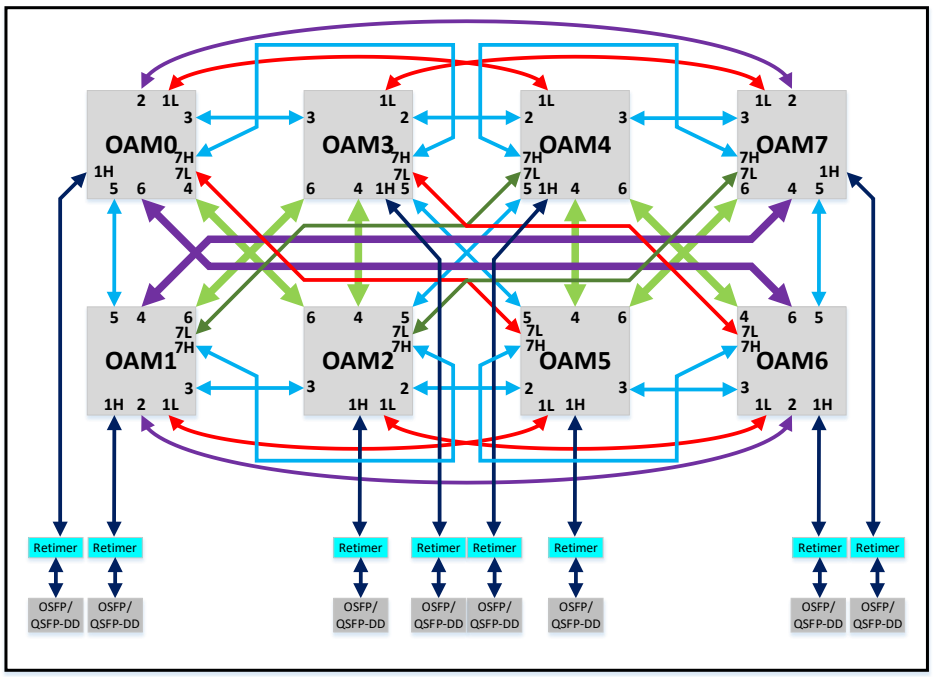


Figure 34 Combined FC/6-Port HCM Topology

Port 1,4,6,7 has a total of 16 lanes, and Port 2,3,5 has a total of 8 lanes in Figure 34:

- Fully connected: 7 x8 links using port 1-7 first x8(1L-7L)
- 2nd half of port 1s(1H) are connected to EXP or on board OSFP/QSFP-DD (scale-out)
- 6 port HCM: all 6 ports are in connector 1 only. x16 link for port 4/6, x8 link(5L) for port 5, and 2nd half of port 7(7H)

Below figure shows the detailed port mapping and routing guide:

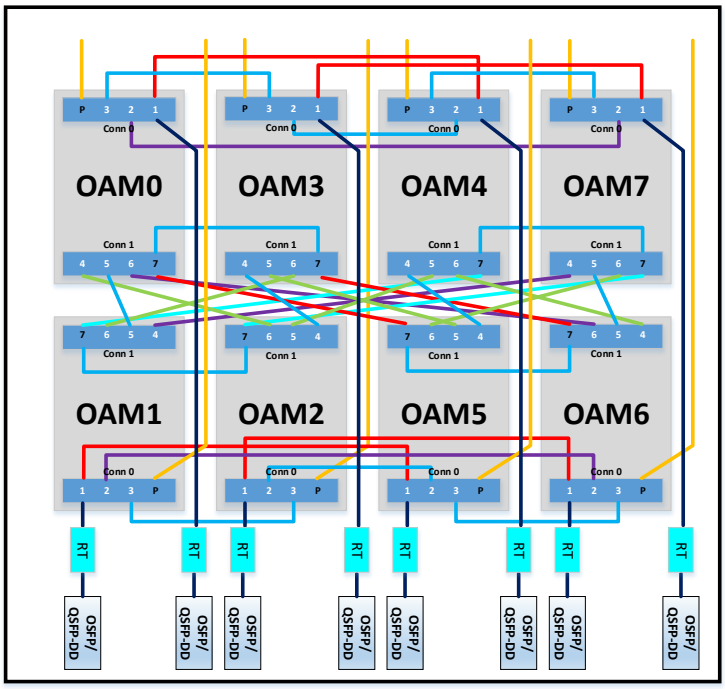


Figure 35 Detail port mapping and routing guidance

Port 4/6(both 4L/6L and 4H/6H), port 5L, 7H are used for 6x8 HCM. This is how it's embedded to this combined topology:

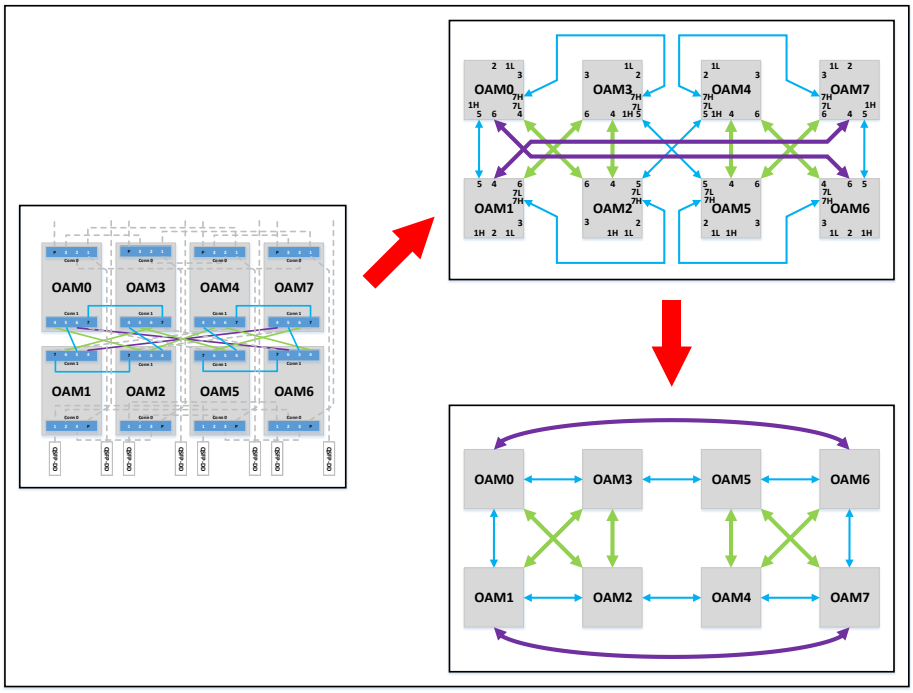


Figure 36 Embedded HCM Topology

9.5. 8-port Hybrid Cube Mesh Topology

Figure below shows an 8 port HCM(Hybrid Cube Mesh) topology of 8 modules in a UBB. Please follow port mapping to design OAM to be able to fit in the UBB. Port 4/6 connects through OSDP/QSFP-DD cables for a single 8 module system. These OSFP/QSFP-DD cables are also used for expansion (scale-out).

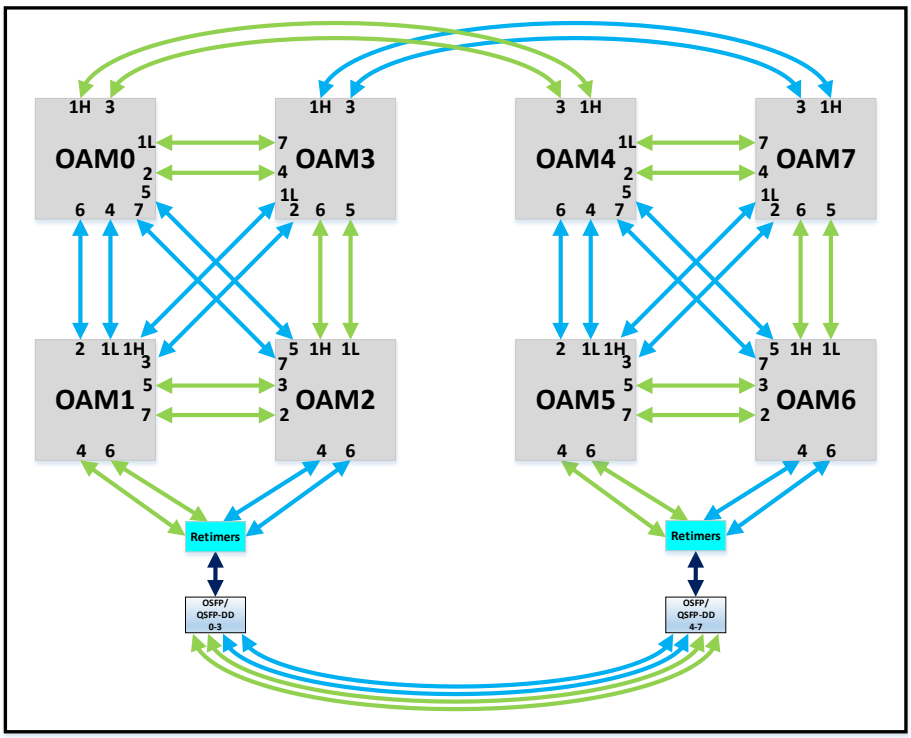


Figure 37 8-port Hybrid Cube Mesh Topology

- links HCM using links: 1, 2, 3, 4, 5, 6, 7.
- SerDes Port 2, 3, 4, 5, 6, 7 are x8 lanes.
- SerDes Port 1 is 2 x8 lanes.
- 1L –Lower 8-bit, 1H –Upper 8-bit.
- Links: 4, 6 (OAM #1, #2, #5, and #6) are used for scale-out, can be connected directly through OSFP/QSFP-DD cables or EXP Module retimers.

Below is the routing suggestion: total 4 layers, two layers for TX, two layers for RX. Port 4/6 are connected through cables.

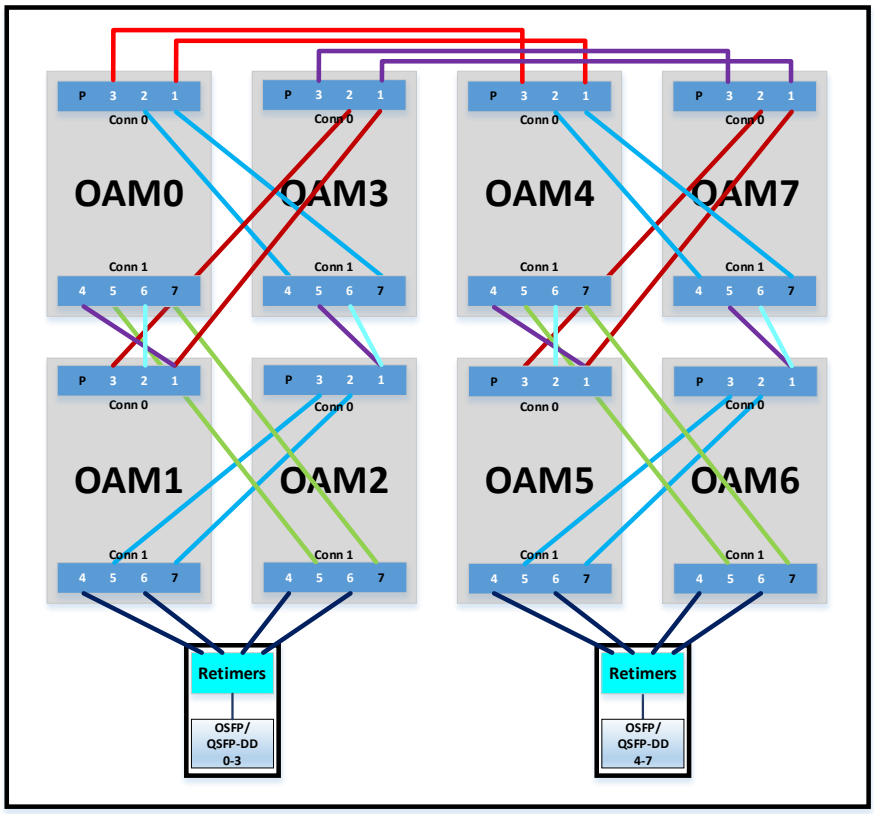


Figure 38 8-port HCM topology routing guide

9.6. 11-Port (7+4) FC/Retimer Topology (Fully Connected + 4 Scale Out)

Figure below shows an example of 11-port topology with seven SerDes ports for fully connected topology and four SerDes ports for scale out (per OAM) of 8 modules in UBB. The scale out ports are routed to EXP modules to support 32 scale out ports. Please follow port mapping to design OAM to be able to fit in the UBB.

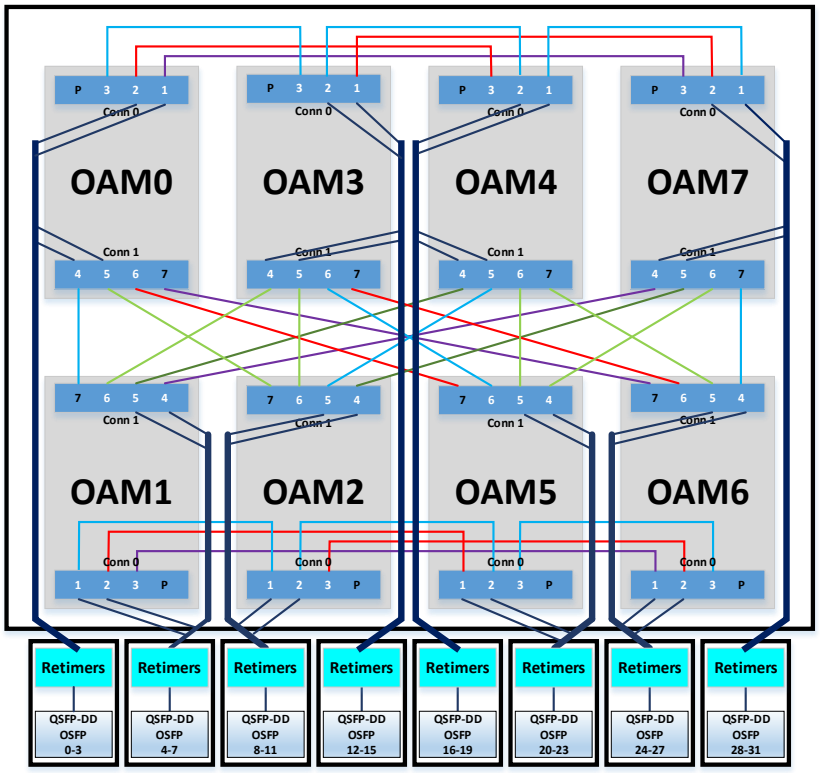


Figure 39 11-Port (7+4) FC/Retimer Topology

- links FC using links: 1, 2, 3, 4, 5, 6, 7
- SerDes Port 3, 6, 7 are x8 lanes
- SerDes Port 1,2,4,5 are 2 x8 lanes
- 1L –Lower 8-bit, 1H –Upper 8-bit

9.7. 8-port Switch-Based Topology

Figure below shows an example of 8-port switch-based topology with eight SerDes ports of each OAM are connected to eight EXP modules to form fully connected topology through switch devices for scale up and out.

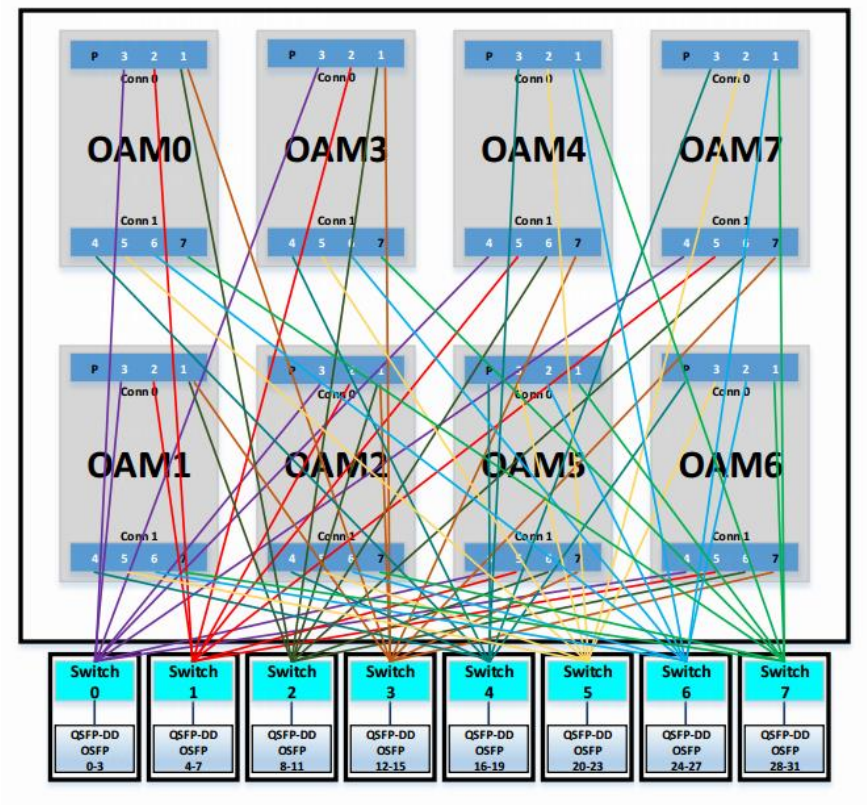


Figure 40 8-port Switch-Based Topology

9.8. UBB silkscreen

OAM silkscreen shall follow module ID naming as OAM0, OAM1, OAM2, et al. EXP silkscreen shall followEXP0, EXP1, EXP2, et al.

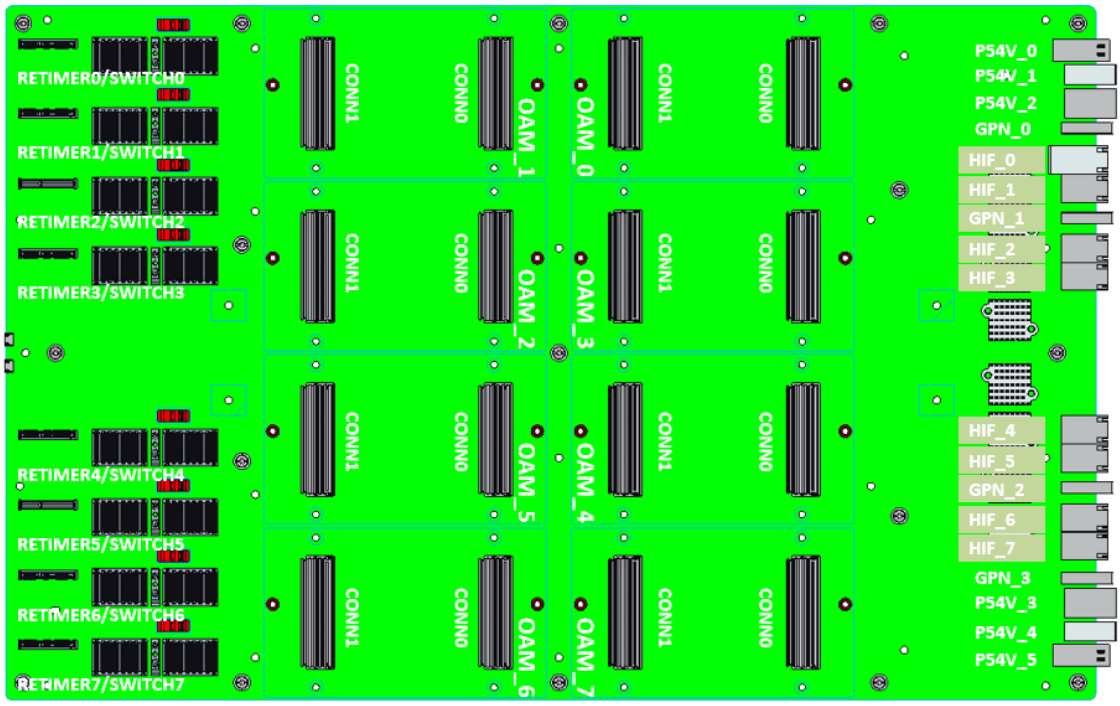


Figure 41 UBB silkscreen example

10. Mechanical Specification

10.1. Board dimension

Board dimension is limited to 655mm x 417mm x 5.0mm (L x W x T). The handle design and interface for the UBB assembly are not defined in this specification and may be customized as needed. The board's outline is fixed as shown in the drawings and may not be altered or customized.

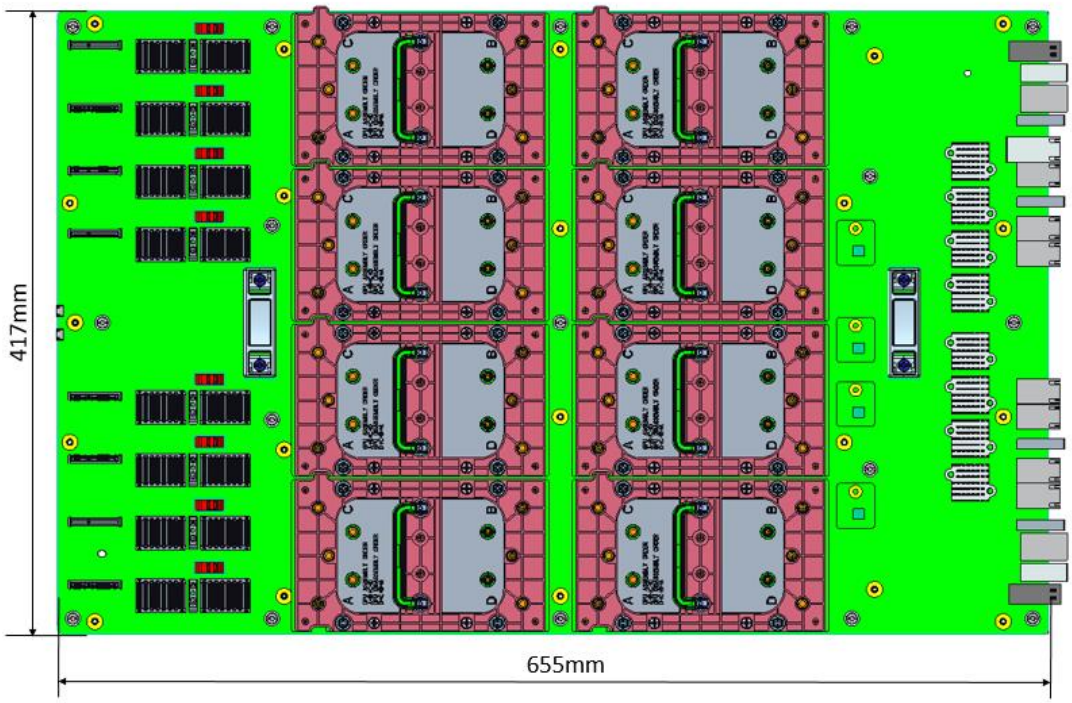


Figure 42 UBB board dimension

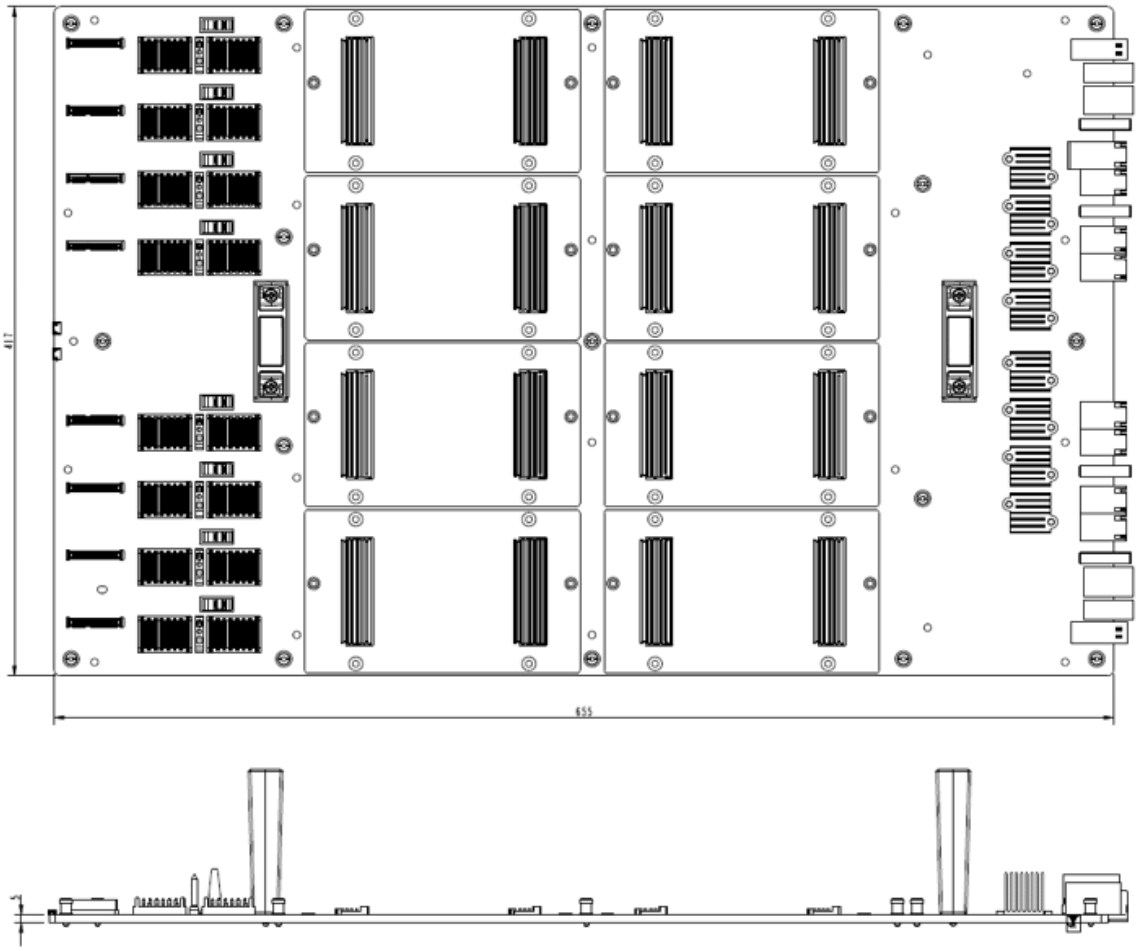


Figure 43 UBB board Top and side views

10.2. Required Components

10.2.1. OAM Placement / Mirror Mezz Pro Connectors

There are two different topologies with different connector orientations. Figures below highlight connector numbers and pin 1 locations to distinguish the two architectures.

FC (Fully connected)

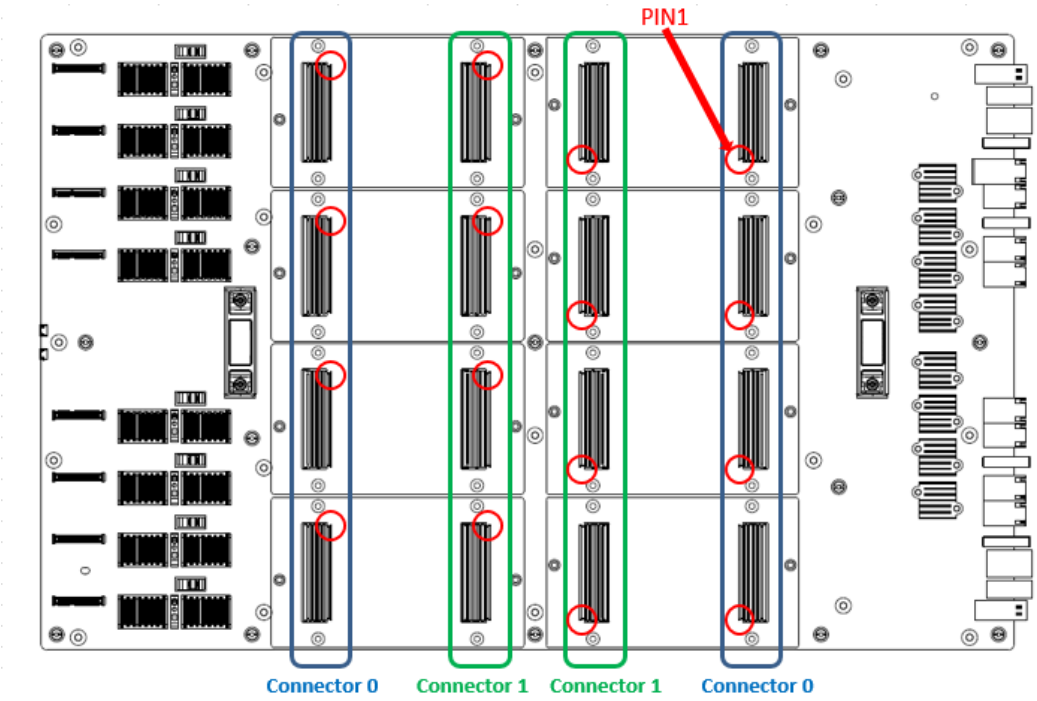


Figure 44 OAM Mirror Mezz Pro connector pin1 FC orientation

HCM (Hybrid Cube Mesh) connection

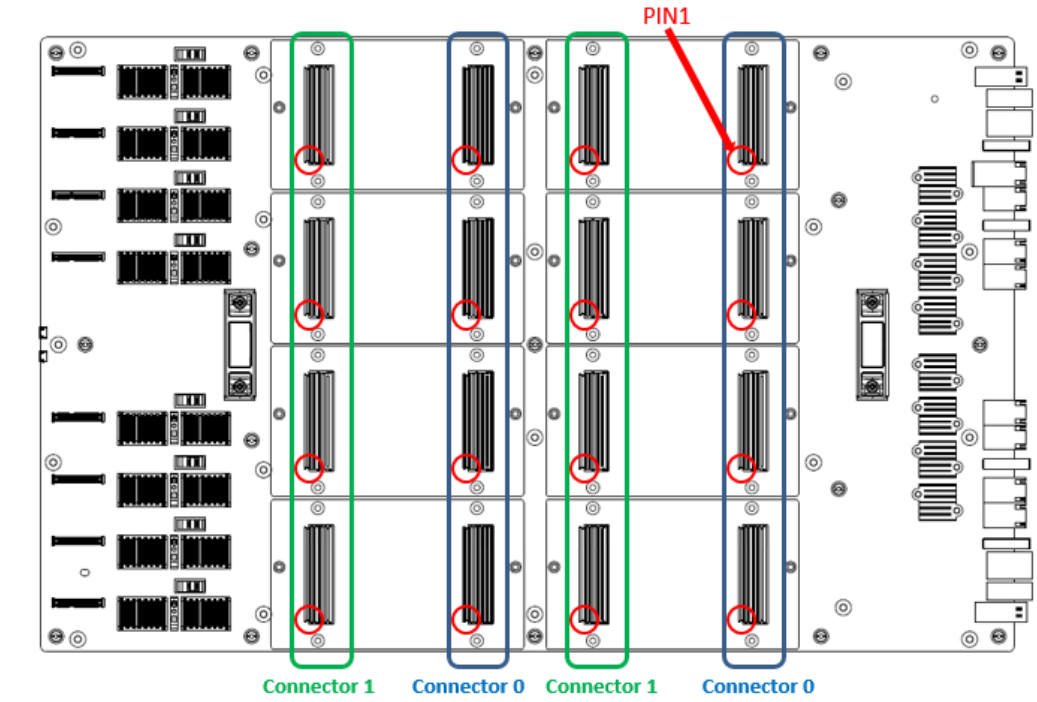


Figure 45 OAM Mirror Mezz Pro connector pin1 HCM orientation

10.2.2. I/O Connectors

Multi-system scale-out with QSFP-DD connectors. Two Micro USB connectors are also exposed from the UBB to the exterior of the chassis for debugging.

Table 26 UBB IO connectors

Item	Vendors	Model number	Descriptions
3	Molex	105017-0001	Micro USB Connector

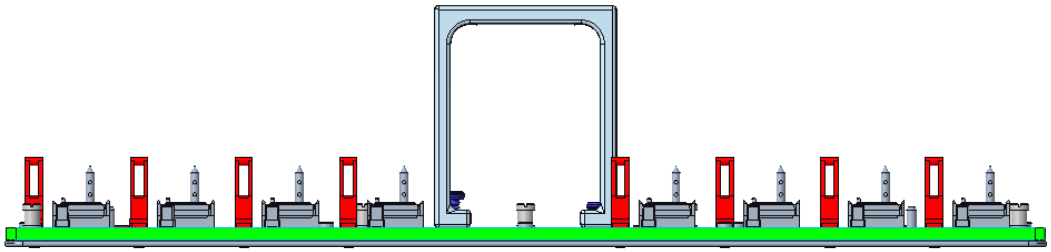


Figure 46 UBB Front IOs

High speed and Power Connector

Table 27 High speed and Power Connector

Item	Vendors	Model number	Descriptions	Qty
1	Amphenol	10137002-101LF	High Density Connector	7
2	Amphenol	10131762-301LF	High Density Connector	1
2	Amphenol	10037909-101LF	Guide Pin	4
3	Amphenol	10061289-001LF(2x3)	54V Connector	2
	Amphenol	10028917-001LF(2x2)	54V Connector	2
4	Amphenol	10136689-003LF	54V Connector	2

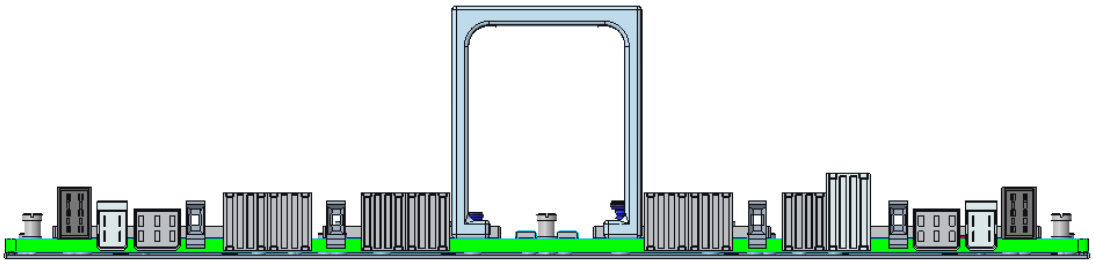


Figure 47 UBB high speed and power connectors to HIB

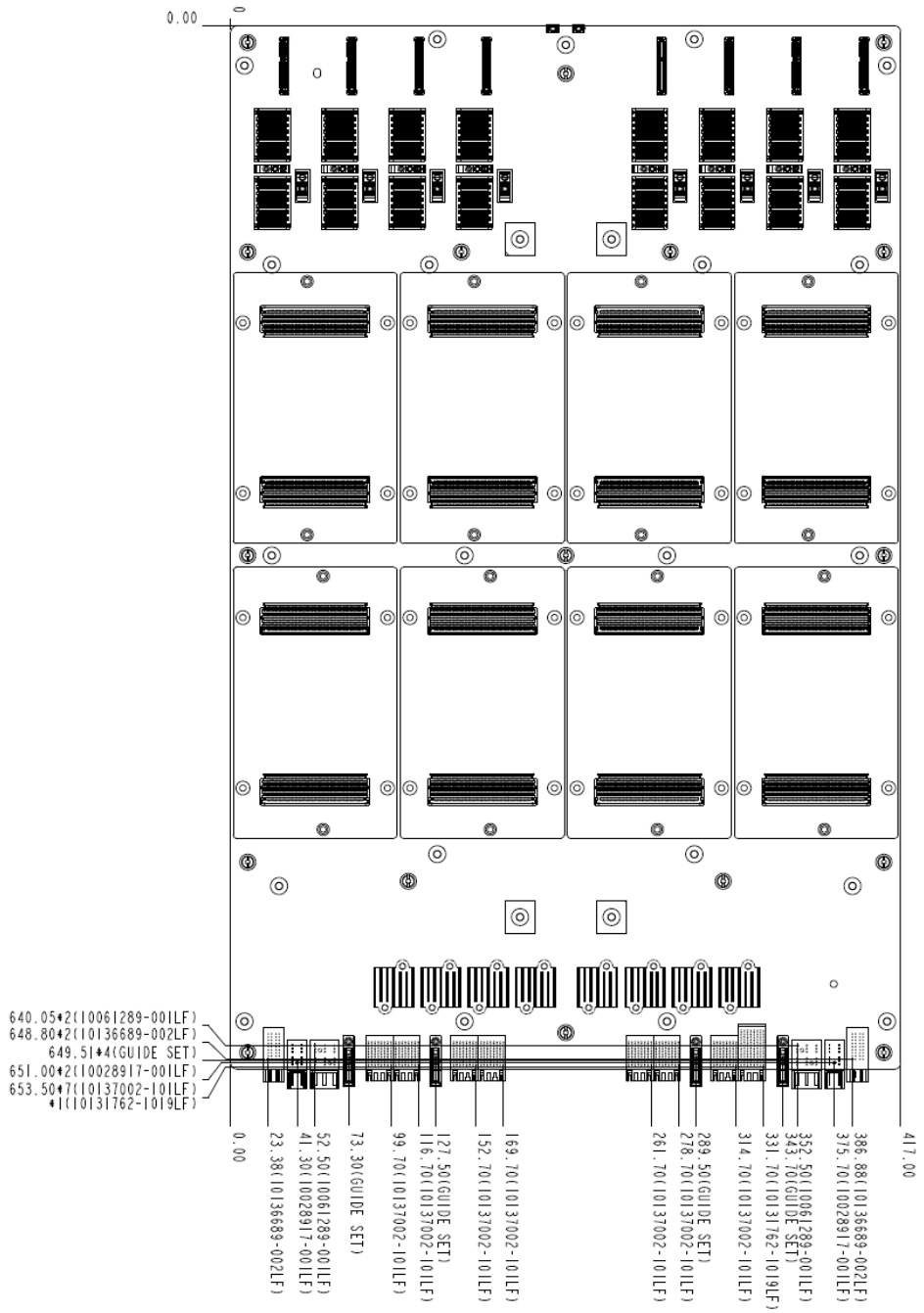


Figure 48 UBB high speed and power connectors coordinate

10.2.3. Screw Mounting Holes

This chapter defines the screw hole sizes and locations. 3D files are on the OCP-OAI Wiki.

Mounting holes to UBB tray :

There are 17 screw mounting holes to secure UBB on the UBB tray.

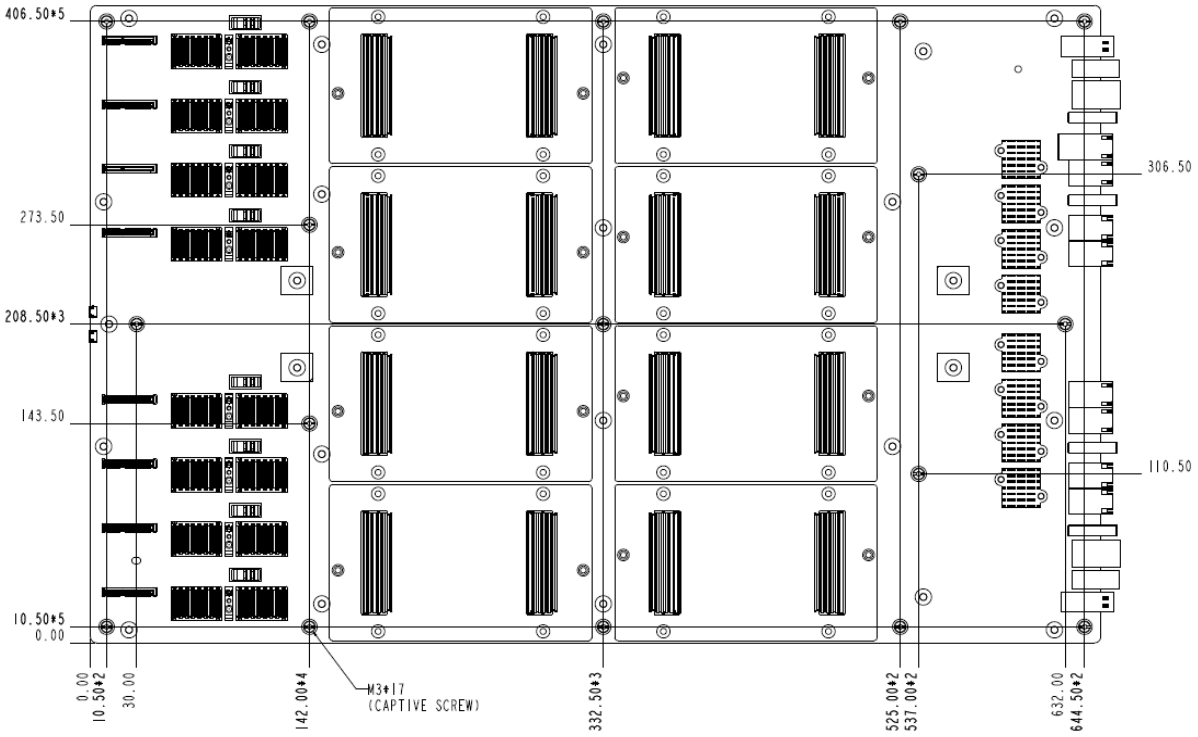


Figure 49 mounting holes

Through holes for OAMs:

There are 32 through holes for OAMs screwing down to bolster.

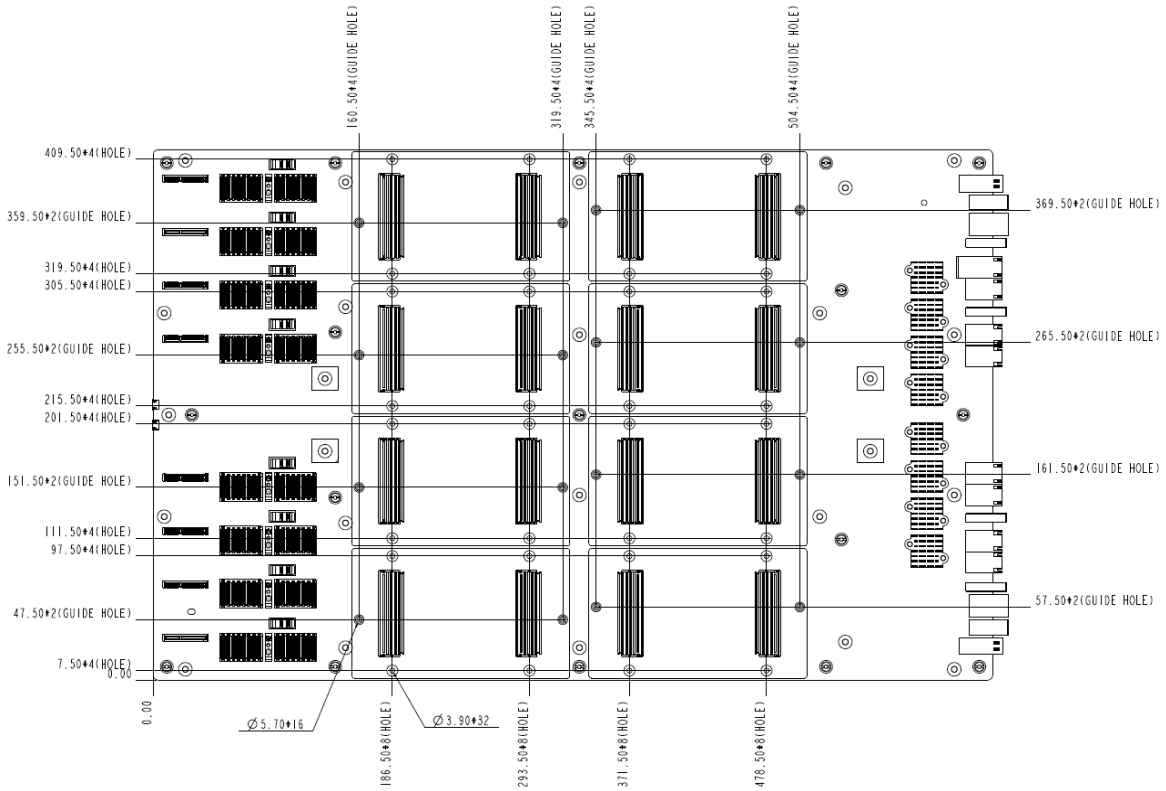


Figure 50 OAM through holes

OAM guide hole (SMT Nut):

SMT nut illustrated below is soldered to UBB at the 5.7mm diameter holes specified in Figure below.

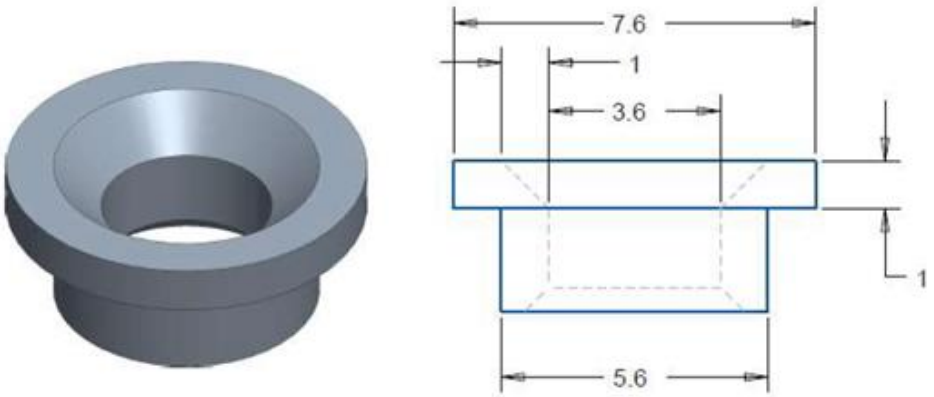


Figure 51 OAM guide hole

Mounting holes for bolster:

There are 2 guide holes to align UBB and bolster first, then 25 mounting holes used for fastening UBB with bolster.

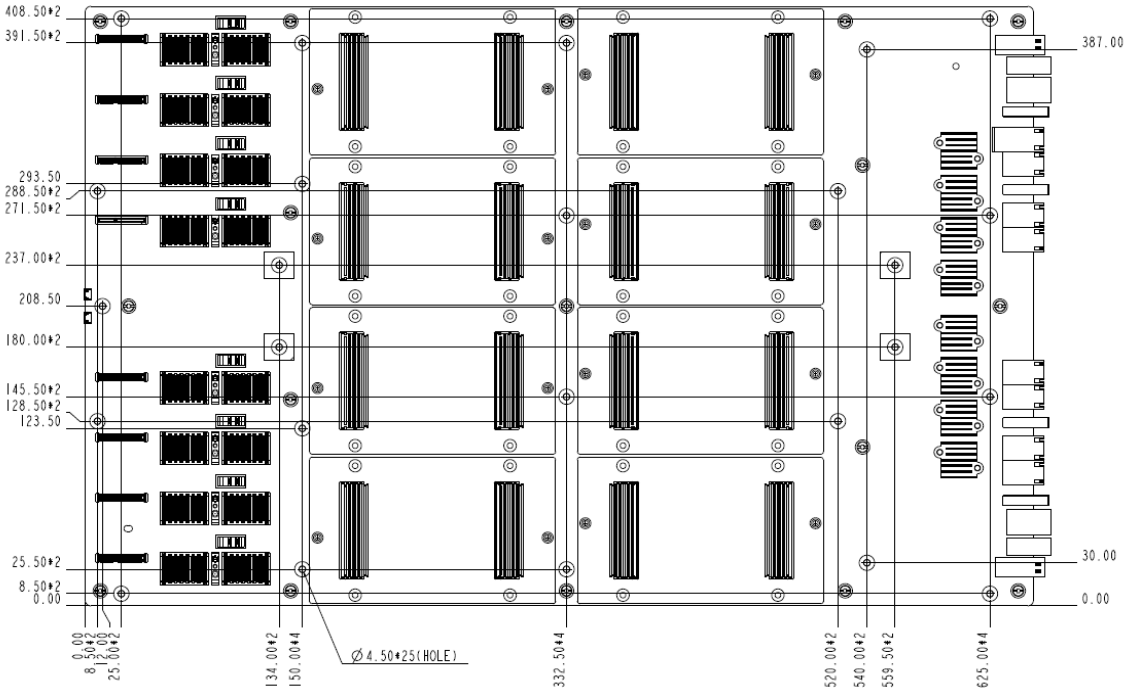


Figure 52 Mounting holes for bolster

10.3. Recommended Components

10.3.1. Air Baffle Holes

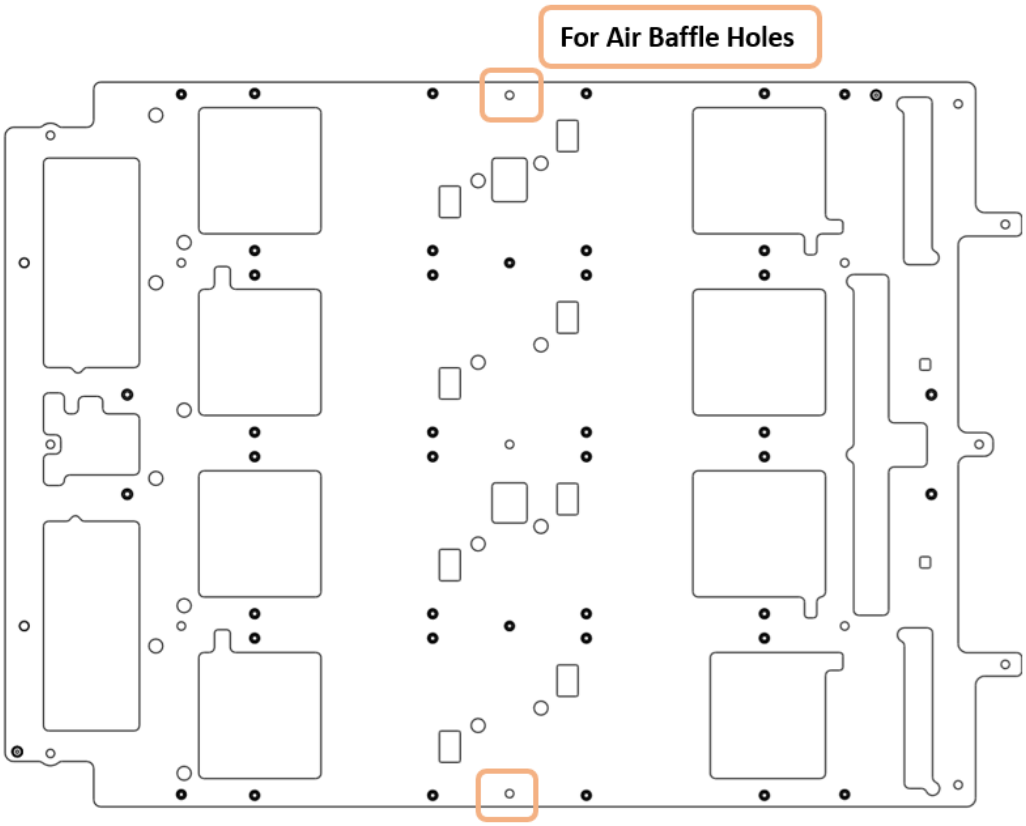


Figure 53 Air Baffle mounting holes on the stiffener

Hole sizes and locations are recommended and can customize for individual needs. The designs are available as part of the 3D package; an air baffle in the system is highly recommended.

10.3.2. UBB Handles

Southco handle (PN: P8-99-236)

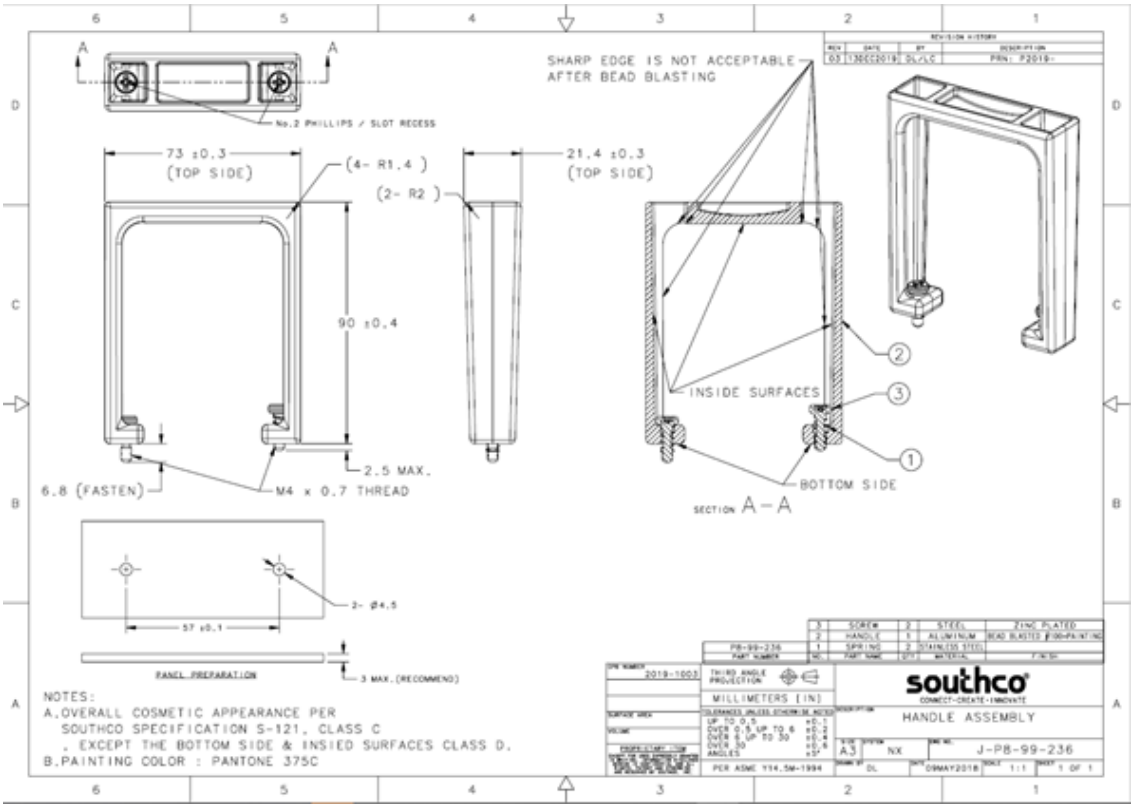


Figure 54 Reference UBB handle

UBB handles are intended for ease of assembly of the baseboard into the system. It is not intended to be used to lift the chassis in its entirety. The system design highly recommends having these handles, and the actual size and type may customize accordingly.

10.4. Assembly

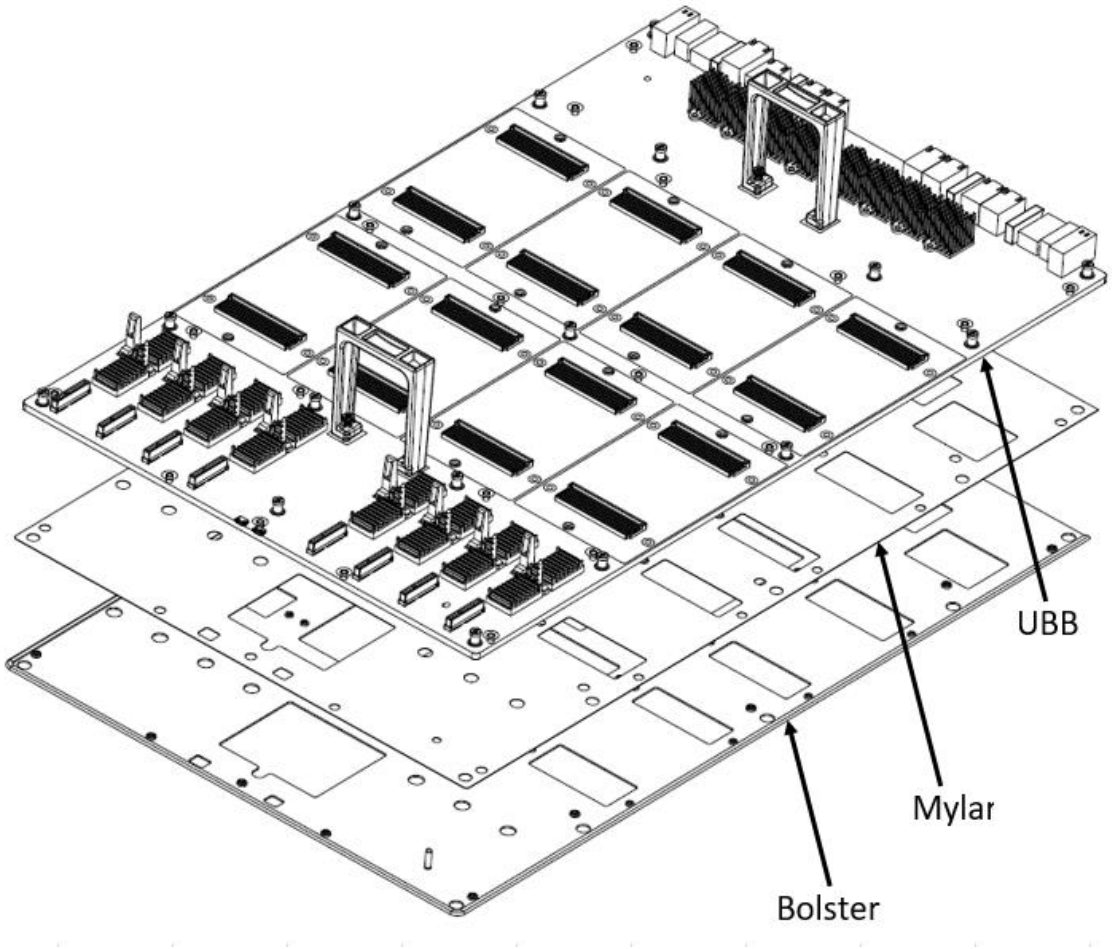


Figure 55 UBB assembly DWG

10.4.1. Screw Torque

Table 28 Screw size and torque spec

Thread Type	Kgf-cm
M3.5	9
#6-32	9
M4	14

10.4.2. Reference Bolster Plate

OAM module, handle with UBB board can be mounted to bolster via mounting screws.

thickness: 4 mm

material: Aluminum alloy

Mounting standoff: #6-32, M3.5 and M4 threaded

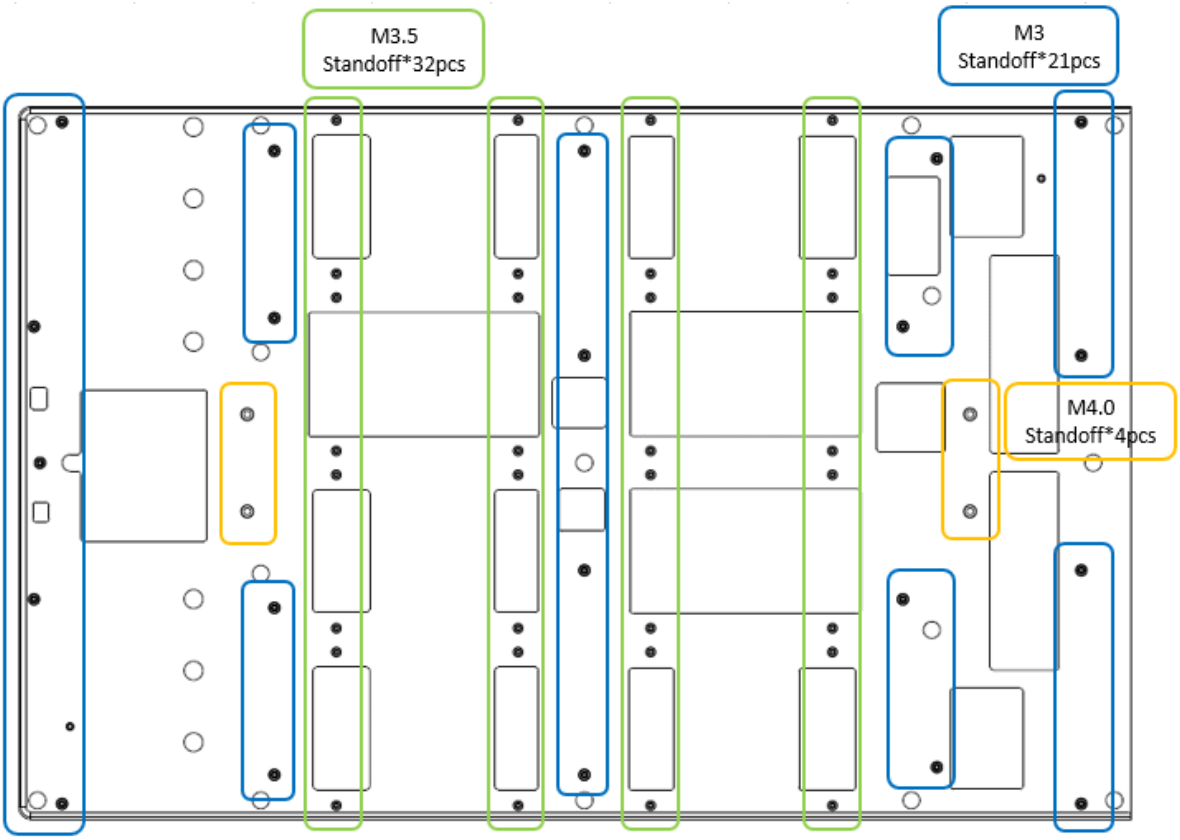


Figure 56 Bolster plate reference design

10.4.3. Mylar

Mylar insulators located between the top and bottom bolster and UBB surface

thickness: 0.25 mm(include adhesive)

material: PC1870A/EFR85(reference)

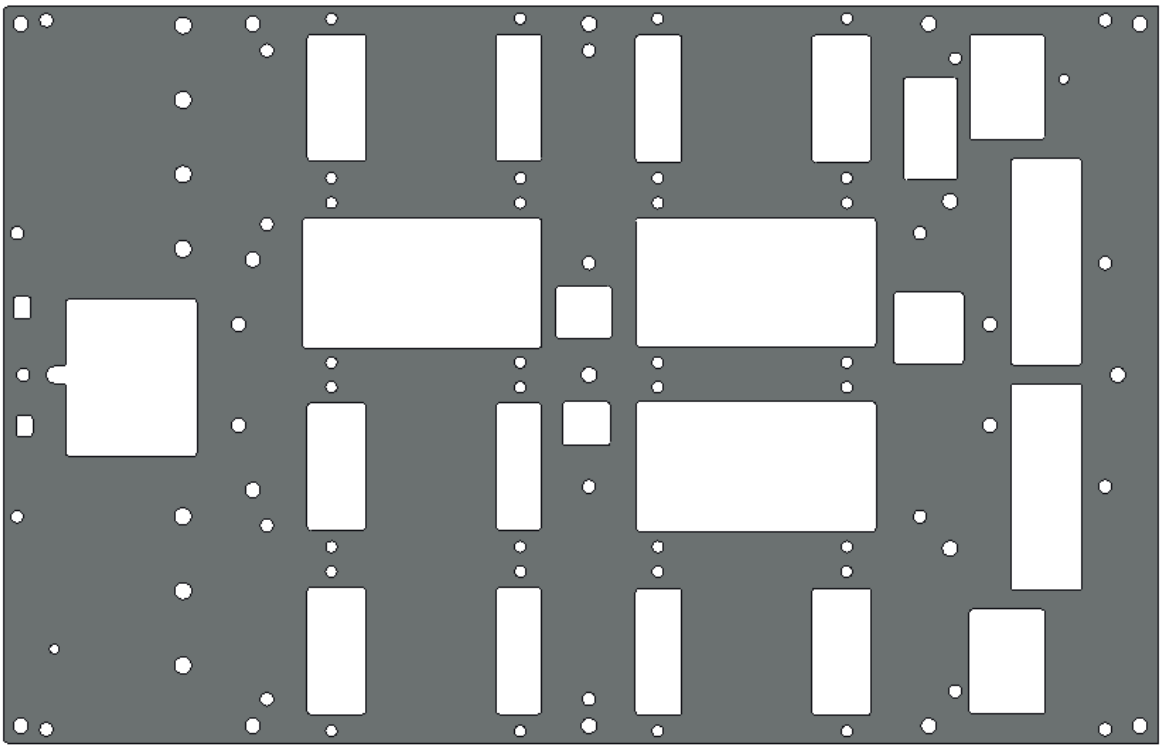


Figure 57 UBB mylar

11. Thermal and Environmental Specification

11.1. Environmental Conditions

To meet the thermal reliability requirement, the cooling solution should dissipate heat from the components when the components on UBB are operating at their thermal design power. OAM and UBB should be able to work in the following environmental conditions without any throttling or thermal issues:

- Ambient temperature: 5°C to 35 °C
- Board surface approach temperature: 10°C to 55 °C
- Altitude: sea level to 3000 ft*, without temperature derating
- Relative Humidity: 20% to 90%

*: support altitude up to 6000ft is recommended

Cold boot temperature: the module should be able to boot and operate at an initial temperature of 10°C

In addition, the UBB should remain unaffected at a non-operational storage temperature range of -20°C to 85°C.

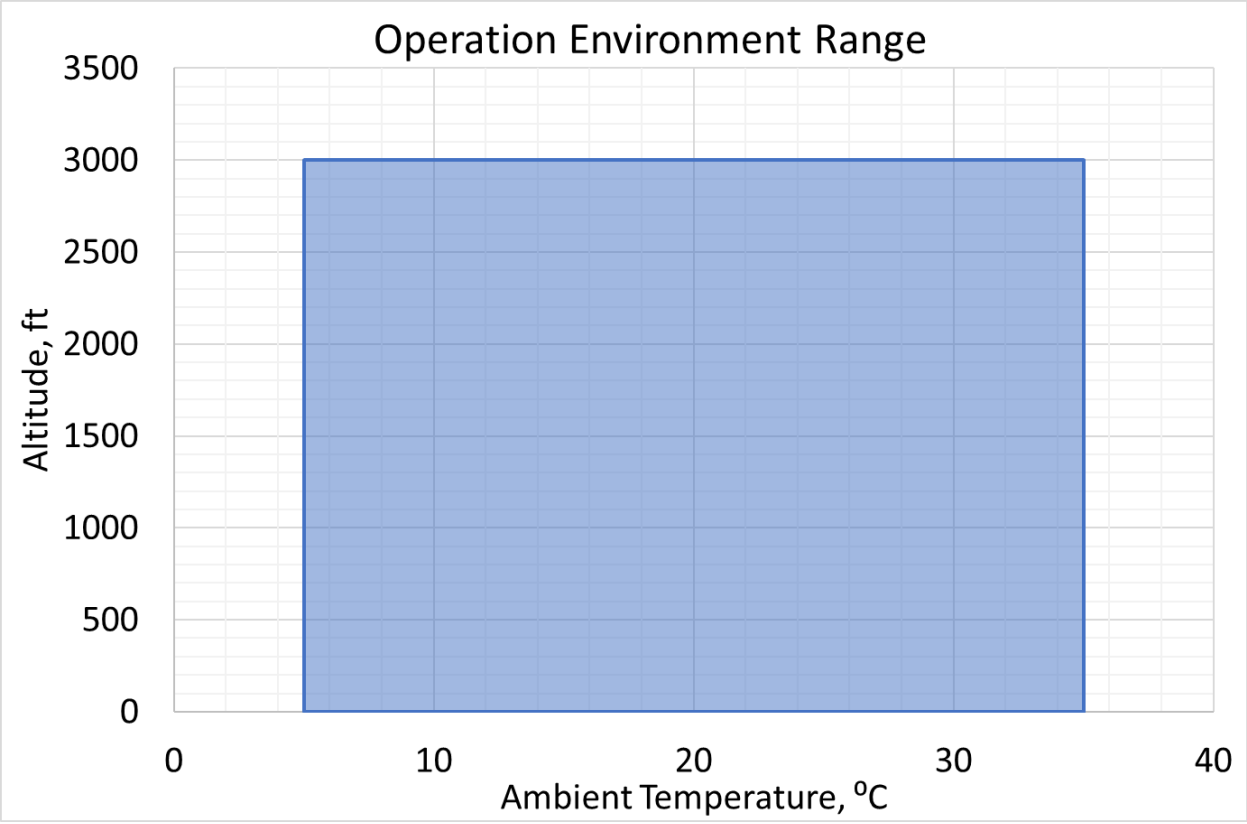


Figure 58 Module Operation Ambient Temperature

11.2. Air Flow Direction

The UBB operates in two different airflow directions, which are:

1. EXPs to OAMs
2. OAMs to EXPs

If the UBB is in airflow direction 1, the downstream OAMs (OAM0/3/4/7) and retimers might become thermally critical; if the UBB is in airflow direction 2, the QSFP/OSFP connectors on EXP might become thermally critical.

For user scenarios with optical transceivers on the EXP card for scale out, it is recommended to adopt airflow direction 1 to provide fresh air for EXP cooling. Preliminary assessment on airflow direction 2 shows that it becomes difficult to support the optical transceivers on EXP cards due to preheat from OAMs, and limited space for heatsinks.

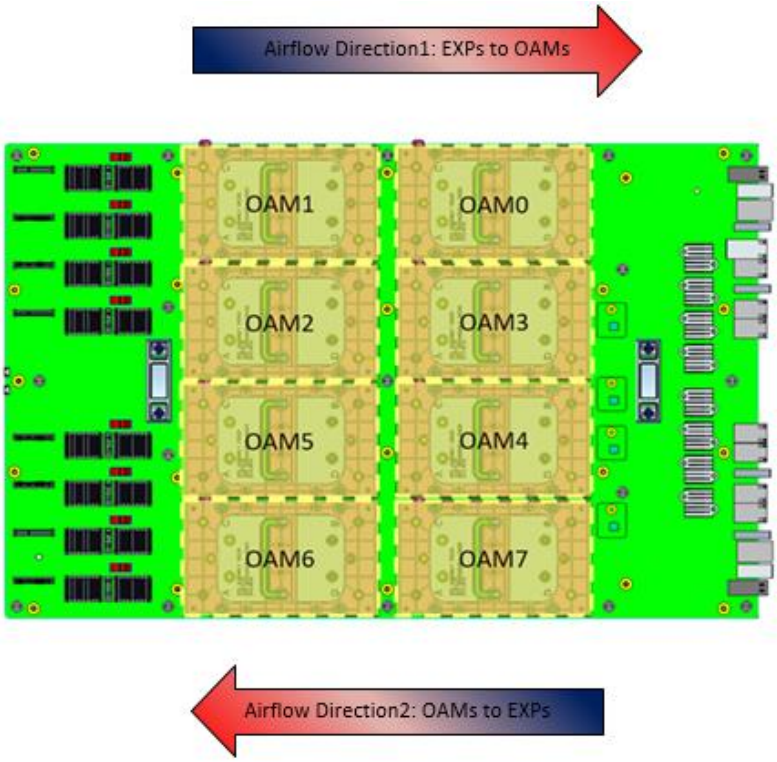


Figure 59 UBB at different airflow directions

11.3. Keep Out Zone

The heatsink manufacturing process such as diecasting and punching may have the tolerance lower than 0.3mm for contour, so for the stack-up tolerance, it is recommended that to keep things out from the heatsink boundary at least 1mm away and to prevent placing anything higher than the OAM to keep the heatsink In/Outlet flow area fluently.

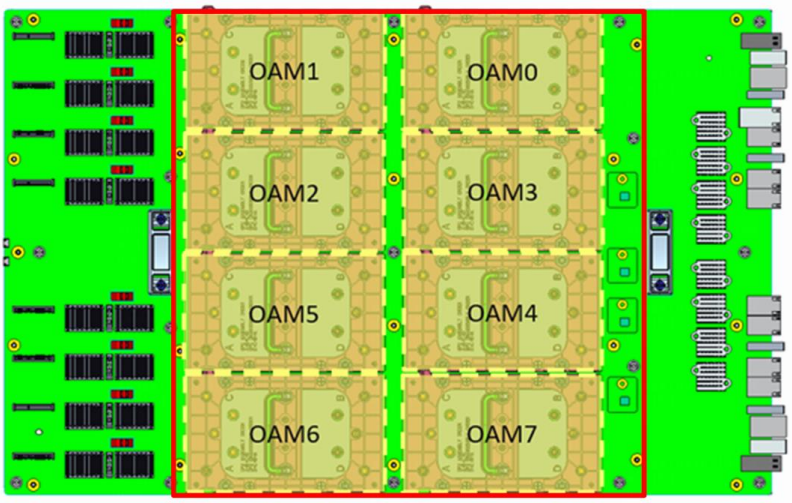


Figure 60 UBB heatsink recommended airflow area keep out

Extrude w/ push pin heatsink for small chips, and the tolerance will be about +-0.3mm. It is recommended to follow the 1mm keep out, and the height limit needs to make sure everything under the heatsink is lower than the OAM height, preventing to cover the area over heatsink for better assembly space and cooling.

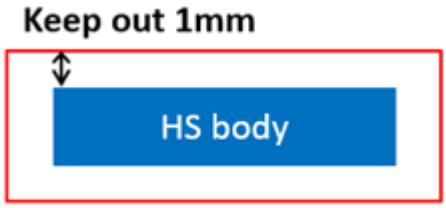


Figure 61 small heatsink keep out

11.4. Temperature Report

The local ambient sensor on UBB board for Air cooling control or protecting shutdown, there is 6 sensors location for reference to monitoring the upstream and downstream flow, may base on the system requirement to choose the sensor location and quantity, sensors need to support both UBB downstream and upstream placement. And main inlet temperature sensor requirement is better to keep accuracy at ±3°C. The encountered accuracy is generally better than this. This inlet sensor should locate at the front end of the UBB board.

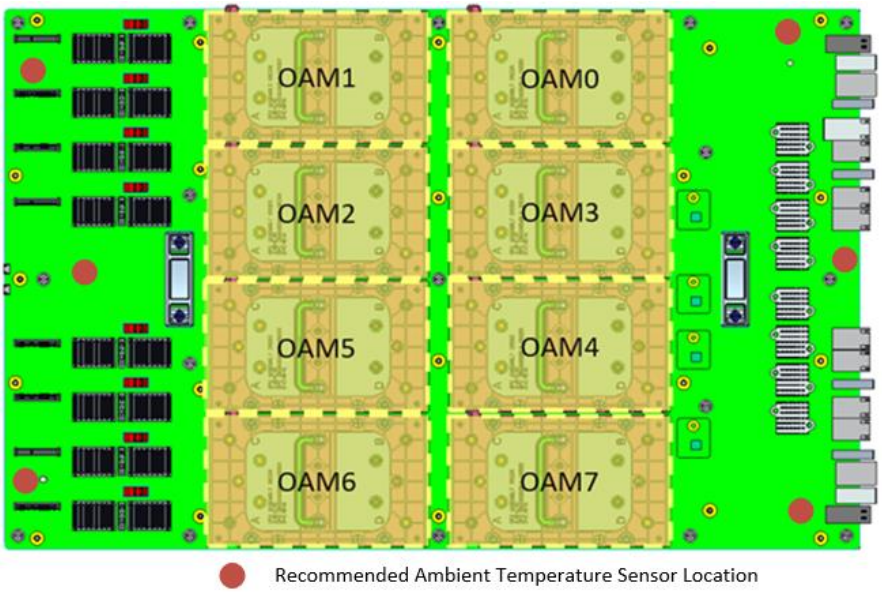


Figure 62 Recommended Ambient Temperature Sensor Map

If any sensitivity components cannot feedback themselves, they will need an extra sensor nearby to ensure the location can reflect the needs of the area of the system they want to protect. They shall be placed as required to provide adequate protection for each major section of the system, such as re-timer, QSFP-DD/OSFP, and try to avoid power trace or something hot nearby. If the heat source cannot be avoided, the sensor must be inserted vertically.

The temperature sensor reading needs to be carefully calibrated for the operating temperature range specified in section 11.1 at different stress conditions. It's recommended to use a 'standing' type temperature sensor instead of a surface-mounted type, and keep a significant distance from heat sources, to avoid impact from adjacent heating.

For components of significant power consumption on the board, including OAMs, EXP Modules, retimers, etc., their temperatures are expected to be reported with appropriate accuracies and enabled for Fan Speed Control in system BMC.

11.5. Thermal Recommendation

11.5.1. Airflow Budget

It is recommended that the UBB module (contains 8*OAM and other onboard hardware like retimer/switch, etc.) operates with full performance should be at or lower than airflow/power ratio of 0.158 CFM/W with an ambient temperature of 35°C at sea level. It is equivalent to an inlet/outlet air temperature increase of 20.2°F/11.2°C.

To keep downstream airflow meet 55°C standard PCIe spec. Maximum inlet/ outlet temperature rise of UBB shall not be more significant than 20°C at 35°C sea level.

- For operation at altitude, the same air temperature difference of 20.2°F/11.2°C or higher is recommended.
- Airflow (CFM) is defined as the total airflow supplied across UBB.
- Power (Watts) is defined as the max total power of all components on the UBB, on the same plane as the UBB (upstream/downstream components).

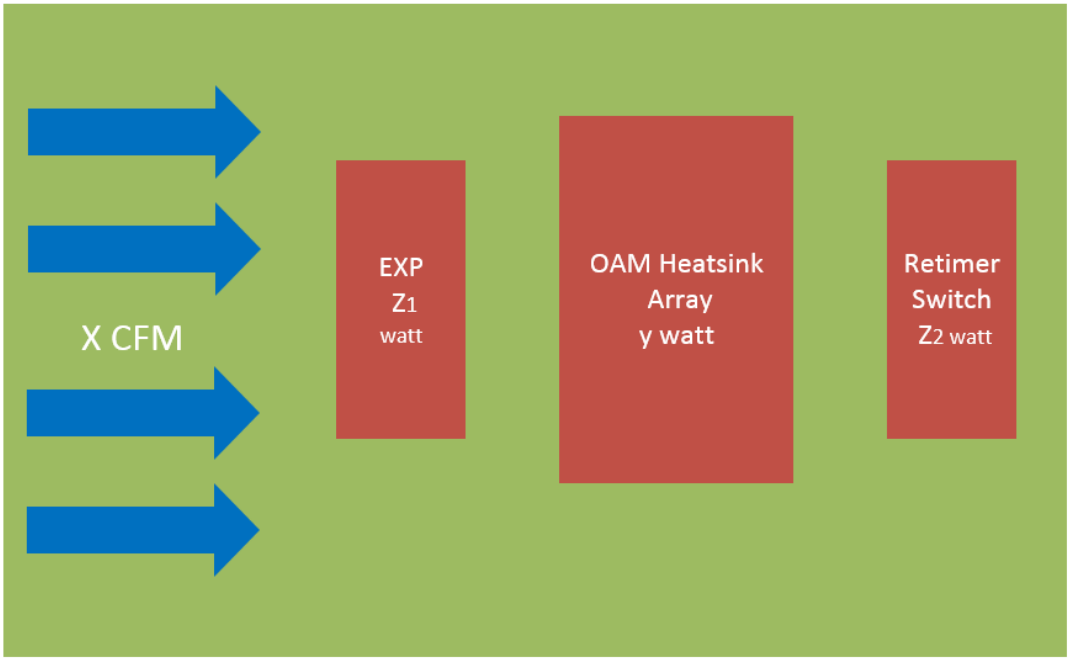
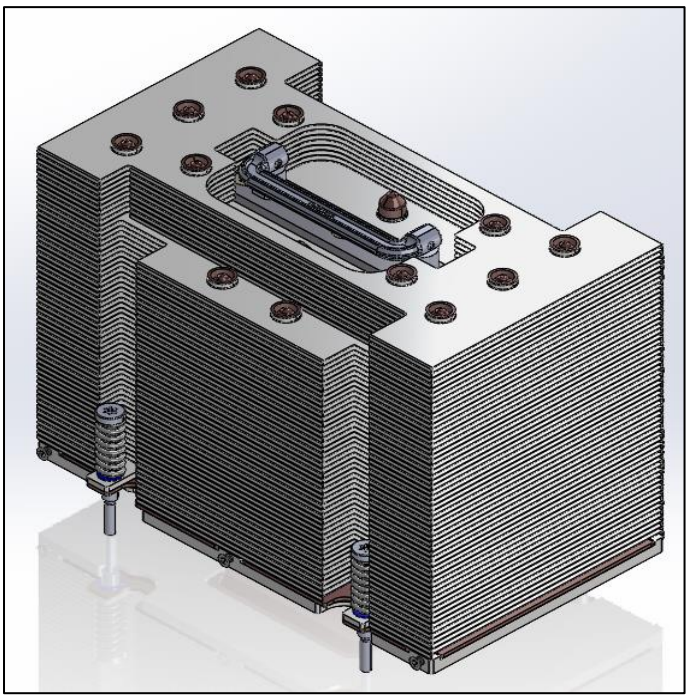


Figure 63 CFM per Watt definition for UBB

11.5.2. Reference Air Cooling Design



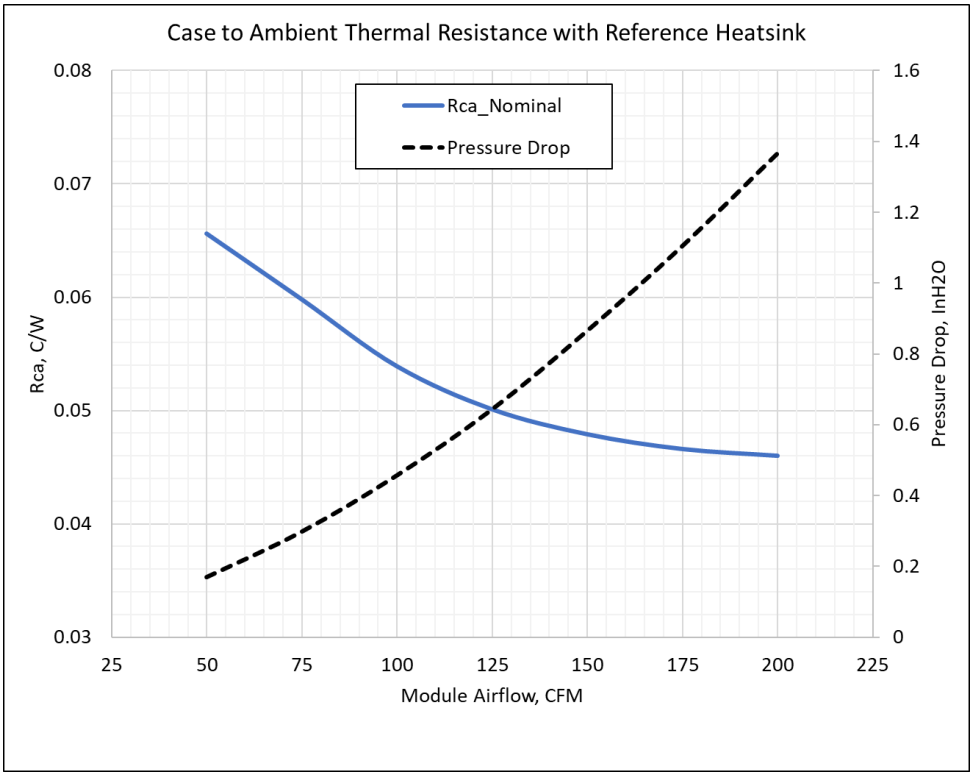
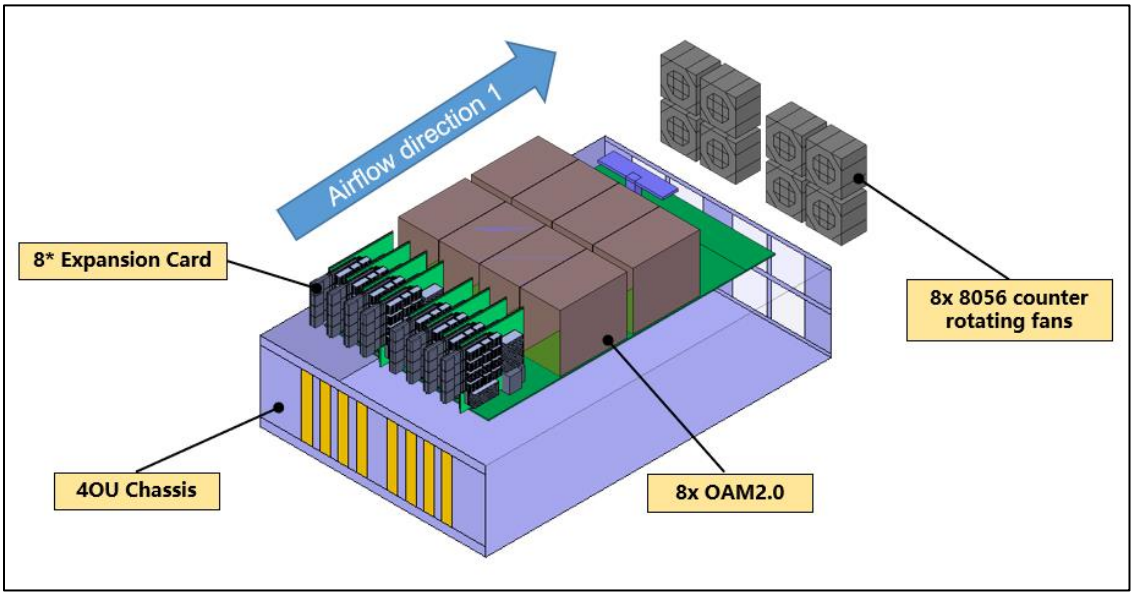


Figure 64 Reference OAM Heatsink with 3D-VC technology

Adopting the OAM reference heatsink (Figure 64) , 4OU reference chassis design, 8x 80mm counter rotating fans and airflow direction 1 (EXP-to-OAM), the total pressure drop, and fan power consumptions are estimated as in Figure below, based on CFD analysis. Based on this analysis, as airflow rate approaches 800CFM, the system fan power consumption will reach almost 1000W, with pressure drop approaching 3 InH2O. We consider 800CFM to be upper limit of reasonable airflow delivery, for such reference system.



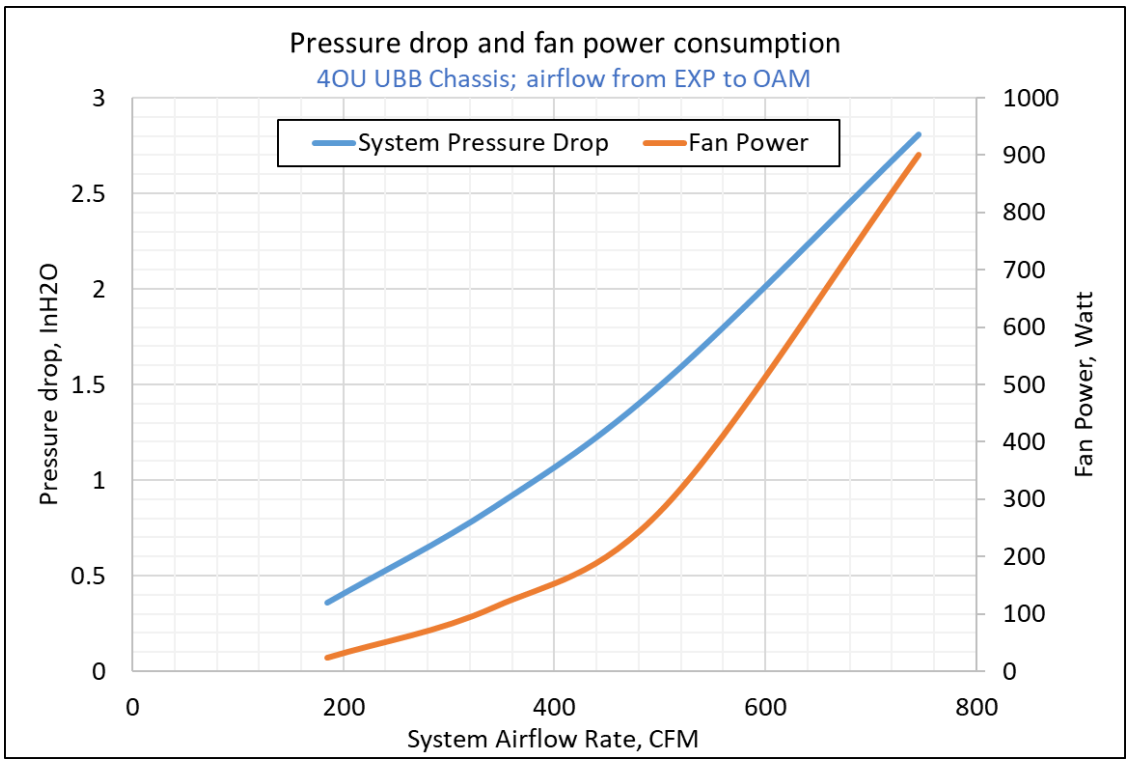


Figure 65 CFD model of the reference 4OU UBB2.0-based platform; pressure drop and fan power consumption for various airflow rates

With system airflow of 800CFM, it is likely capable of cooling 600W OAMs at AMB=35°C and sea level, assuming 150W per EXP card, airflow direction EXP-to-OAM, and a target limit for OAM package surface temp at 80°C. As UBB airflow rate reaches beyond 800CFM, approximately 200CFM per OAM heatsink, the cooling performance of heatsink starts saturating and provides diminishing return. It is still possible to extend the air-cooling capability further, by increasing airflow rate and reducing preheating, which is speculated to require either taller chassis to accommodate more fans or increasing fan power exponentially.

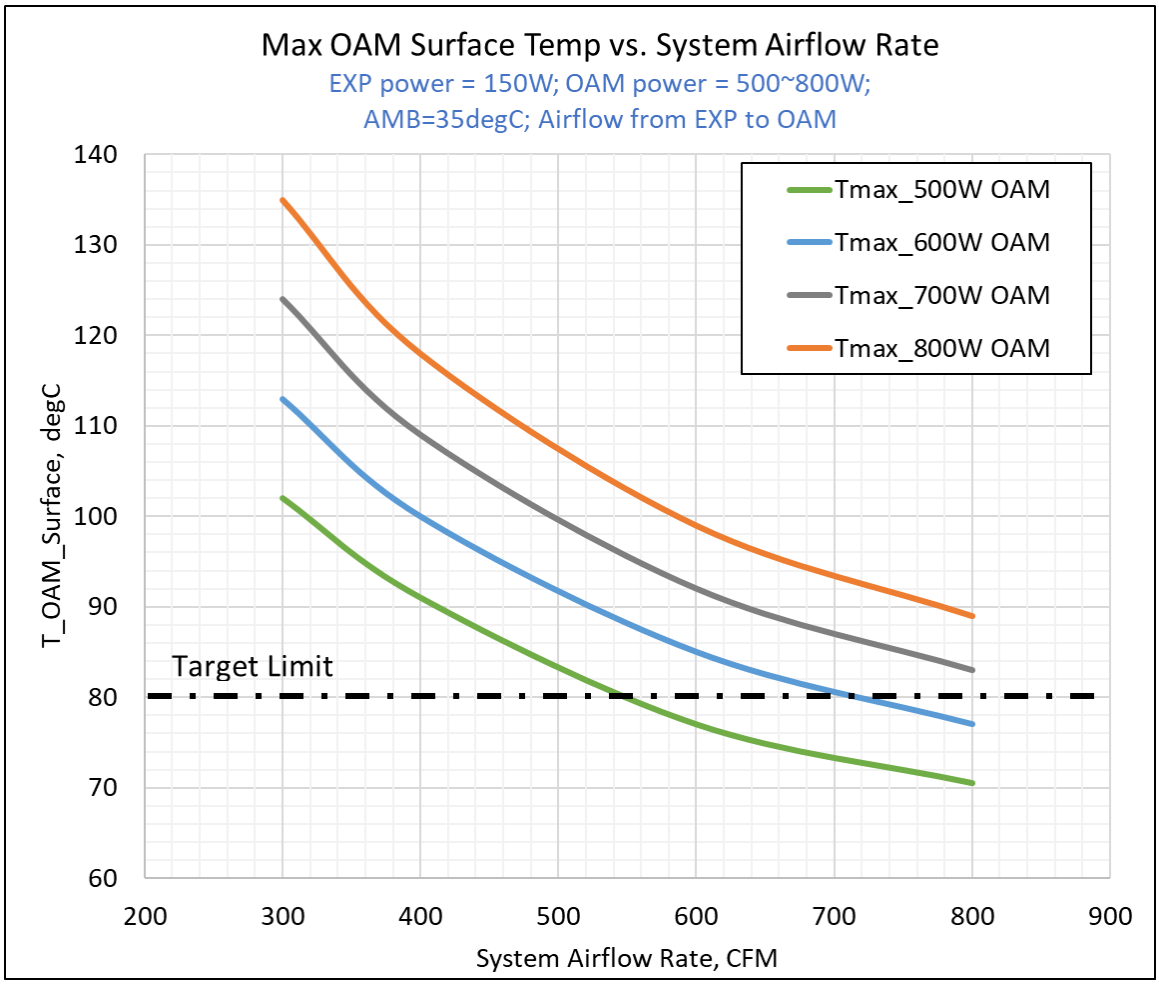


Figure 66 Max surface temperature of hottest OAM in the UBB2.0 system, at AMB = 35degC, sea level, airflow direction EXP-to-OAM, with various airflow rates and OAM power. Many assumptions apply to this analysis.

On the other hand, when airflow direction is from OAM-to-EXP, the thermal risk evaluation will be more complicated as components on EXP card, such as optical transceivers, are likely to become the bottleneck. Analysis for this type of scenarios is still WIP, while we consider liquid cooling OAMs will help address such risk effectively.

11.6. Reference Liquid Cooling Design

A reference system level liquid cooling solution is demonstrated in Figure 66. The cold plate loop consists of 8x OAM cold plates in parallel flow, which removes preheat, lower the flow impedance, and maximize cooling performance for OAMs. In nominal conditions, we expect such solution to be capable of supporting 1kW OAM product cooling, with 30°C coolant (Water or PG25) supply temperature and flow rate of 10 LPM or higher per chassis. A variety of dependencies apply though.
More guidelines around OAI liquid cooling are provided in this publication:

- OAI Liquid Cooling Guidelines:
    - https://www.opencompute.org/documents/oai-system-liquid-cooling-guidelines-in-ocp-template-dec-7-2022-1-pdf

From OCP CE Cold pate group, there are also multiple guidelines published to help cold plate-based liquid cooling solution development for general hardware products:

- OCP ACS Cold Plate Leak Detection and Intervention
    - https://www.opencompute.org/documents/acs-cold-plate-leak-detection-and-intervention-white-paper-pdf-1
- OCP ACS Liquid Cooling Cold Plate Requirements
    - https://www.opencompute.org/documents/ocp-acs-liquid-cooling-cold-plate-requirements-pdf
- OCP Cold Plate Development and Qualification
    - https://www.opencompute.org/documents/ocp-cold-plate-development-and-qualification-with-integrated-comments-pdf

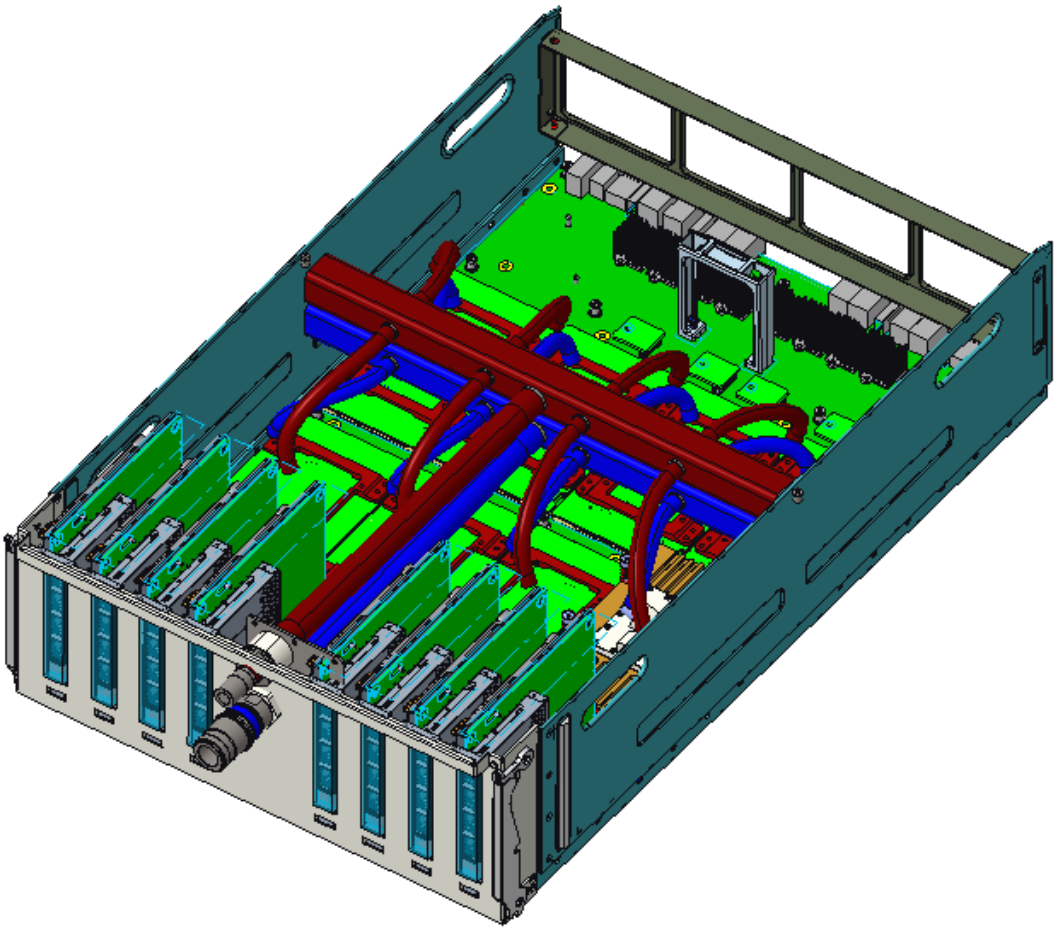


Figure 67 Reference Liquid Cooling Design for UBB. 1: Universal Base Board; 2: Host Interface Board; 3: Power Distribution Board; 4: Liquid Cooling Module. The cooling components and OAMs in the figure are just for concept demonstration and do not represent real solutions.

11.7. Consideration for Immersion Cooling

Immersion cooling is another advanced cooling technology that could bring performance benefit. However, the impact on various aspects are still yet to be examined, including material compatibility, signal integrity, hardware design philosophy, reliability and serviceability, facility design, etc. A series of guidelines have been released by OCP CE Immersion group, to help development of immersion-based hardware products on multiple, but not all areas yet:

- Material Compatibility in Immersion Cooling
    - https://www.opencompute.org/documents/material-compatibility-in-immersion-cooling-document-version-1-0-nov-28-2022-1-pdf
- Base spec of immersion fluid
    - https://www.opencompute.org/documents/ocp-base-specification-for-immersion-fluids-20221201-pdf

- Design Guidelines for Immersion-Cooled IT Equipment
    - https://www.opencompute.org/documents/design-guidelines-for-immersion-cooled-it-equipment-revision-1-01-pdf

12. System Management

12.1. UBB I2C Topology

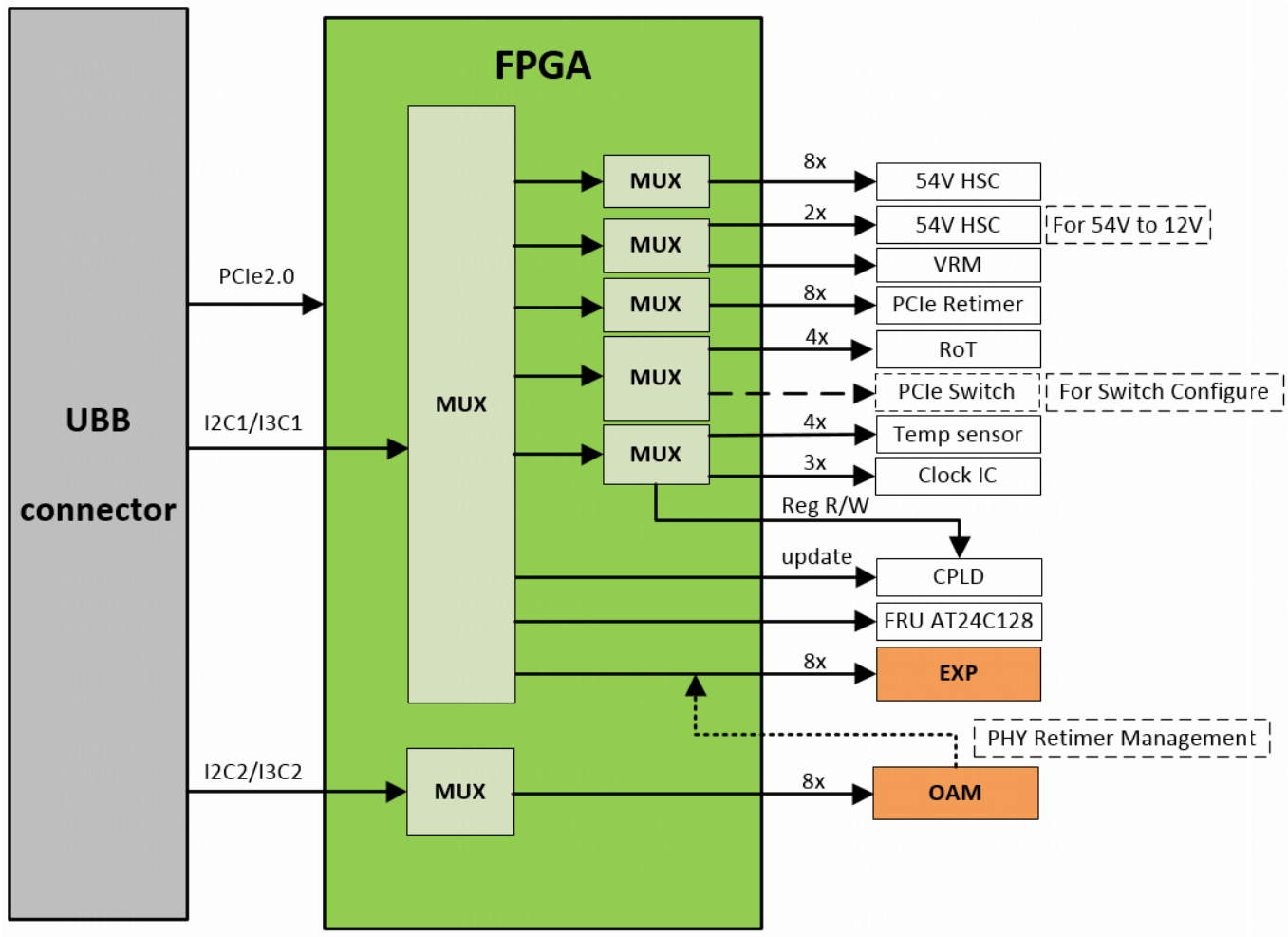


Figure 68 UBB I2C Topology

12.2. Sensors and Events

SEL Definition List

Table 29 SEL Definition List

Term	Full Name
LNC	Lower non-recoverable
LC	Lower Critical (Critical low)
LNC	Lower Non-Critical

UNC	Upper Non-critical
UC	Upper Critical
UNR	Upper non-Recoverable
A	Assertion
D	De-assertion
S	Settable (Threshold sensor only)
R	Readable

Table 30 Sensor name and Event table

Sensor Name	Slave Addr.	Event/Reading Type	Event Triggers	Sensor Unit Type code
OAM_TEMP_0 OAM_TEMP_1 OAM_TEMP_2 OAM_TEMP_3 OAM_TEMP_4 OAM_TEMP_5 OAM_TEMP_6 OAM_TEMP_7	** Define by OAM vendor.	Threshold – 01h	9h: Upper critical going high (A, D, S, R)2h: Lower critical going low (A, D, S, R) A=2204 D=2204 R=1212	Degree C 01h
OAM_ PWR_0 OAM_ PWR_1 OAM_ PWR_2 OAM_ PWR_3 OAM_ PWR_4 OAM_ PWR_5 OAM_ PWR_6 OAM_ PWR_7	** Define by OAM vendor.	Threshold – 01h	9h: Upper critical going high (A, D, S, R) A=200 D=2200 R=1010	Watts 06h
OAM_PRSNT_0 OAM_PRSNT_1	0x80 CPLD	Discrete – 08h	0h: Device Absent 1h: Device Present	Unspecified 00h

Sensor Name	Slave Addr.	Event/Reading Type	Event Triggers	Sensor Unit Type code
OAM_PRSNT_2 OAM_PRSNT_3 OAM_PRSNT_4 OAM_PRSNT_5 OAM_PRSNT_6 OAM_PRSNT_7			<Event Only Type>	
OAM_THERMTRIP_0 OAM_THERMTRIP_1 OAM_THERMTRIP_2 OAM_THERMTRIP_3 OAM_THERMTRIP_4 OAM_THERMTRIP_5 OAM_THERMTRIP_6 OAM_THERMTRIP_7	0x80 CPLD	Discrete – 03h	0h: State Deasserted 1h: State Asserted <Event Only Type>	Discrete 00h
TEMP_INLET_0 TEMP_INLET_1 TEMP_OUTLET_0 TEMP_OUTLET_1	0x90 0x92	Threshold – 01h	9h: Upper critical going high (A, D, S, R) 2h: Lower critical going low (A, D, S, R) A=2204 D=2204 R=1212	Degree C 01h

12.3. UBB FRU Format

There's one FRU EEPROM on the UBB board. FRU is dedicated to BMC.

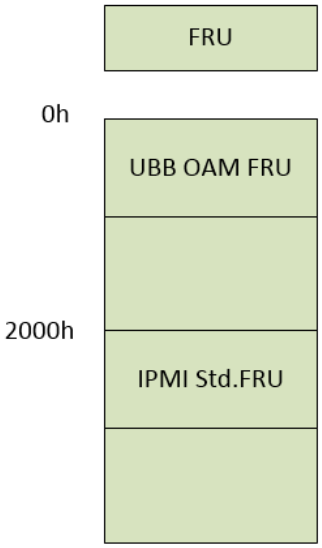


Figure 69 FRU

IPMI standard FRU format: (offset 2000h)

ODM defines the IPMI standard FRU value.

Table 31 FRU content-standard IPMI

Field Name	Value
Board Mfg. Date	Example: "Mon Jan 16 10:33:00 2023"
Board Mfg.	Example: "H3C" "Wiwynn" "Supermicro" "Inspur"
Board Product	"OAI-UBB"
Board Serial	Defined by ODM.
Board Part Number	Defined by ODM.
Board Custom Info 1 for UBB type	String type of following:

	“Retimer” “Switch” “3/4/6 Links HCM” “8 Links HCM” “FC” “FC+6 Links HCM”
Board Custom Info 2 for version	Example: “v1.00”

13. 54V/48V Safety Requirement

13.1. Pollution Degrees

Pollution degrees are classified as follows:

- Pollution degree 1.

No pollution or only dry, non-conductive pollution occurs. Pollution has no influence (example: sealed or potted products).

- Pollution degree 2.

Usually, only non-conductive pollution occurs. Occasionally temporary conductivity caused by condensation must be expected (example: product used in a typical office environment).

- Pollution degree 3.

Conductive pollution occurs, or dry, non-conductive pollution occurs that becomes conductive due to expected condensation (example: products used in heavy industrial environments that are typically exposed to pollution such as dust).

Table 32 Minimum creepage distances

CREEPAGE DISTANCES in mm									
RMS Working Voltage up to and including V	1			2			3		
	Material Group								
	I	II	III	I	II	III	I	II	III
10	0.025	0.04	0.08	0.4	0.4	0.4	1.0	1.0	1.0
12.5	0.025	0.04	0.09	0.42	0.42	0.42	1.05	1.05	1.05
16	0.025	0.04	0.1	0.45	0.45	0.45	1.1	1.1	1.1
20	0.025	0.04	0.11	0.48	0.48	0.48	1.2	1.2	1.2
25	0.025	0.04	0.125	0.5	0.5	0.5	1.25	1.25	1.25
32	0.025	0.04	0.14	0.53	0.53	0.53	1.3	1.3	1.3
40	0.025	0.04	0.16	0.56	0.56	0.8	1.1	1.6	1.8
50	0.025	0.04	0.18	0.6	0.6	0.85	1.2	1.7	1.9
63	0.04	0.063	0.2	0.63	0.9	1.25	1.6	1.8	2.0

13.2. Determination of minimum clearances

For equipment operating more than 2000m above sea level, the minimum clearances should multiply by the factor given in IEC 60664-1.

Table 33 Altitude correction factors

Altitude (M)	Normal barometric pressure (kPa)	Multiplication factor for clearances
2000	80.0	1.00
3000	70.0	1.14
4000	62.0	1.29
5000	54.0	1.48
6000	47.0	1.70

13.3. Creepage and Clearance in Practice

Per OAM spec r2.0, the environmental requirements are operating altitude with no de-ratings

3048m (10000feet)- recommended as this is a Facebook spec and standard for Telco operation.

The clearance distance is about 2.58mm (2.0mm x 1.29) as below condition:

Pollution degree 3 and 63V: 2.0mm

Altitude 4000meter correction factor: 1.29

Please check your SAFETY certification vendor for testing if the clearance can't meet pollution distance and altitude factory.

14. Acronyms

Table 34 Acronyms

Acronym	Definition
ASIC	Application Specific Integrated Circuit
OAM	OCP Accelerator Module
EXP	Expansion Module
RoT	Root of Trust
BGA	Ball Grid Array
BMC	Baseboard Management Controller
TDP	Thermal Design Power
EDP	Excursion Design Power
GPU	Graphic Processing Unit
MPN	Manufacturing Part Number
DXF	Drawing eXchange Format
PCBA	Printed Circuit Board Assembly
UBB	Universal Baseboard
OAI	Open Accelerator Infrastructure

15. Version History

Table 35 Version History

Author	Description	Version	Date
Song Kok Hang (Meta) Ahmed AbouAlfotouh (AMD) Cheng Chen (Meta) Anthony Chan (Meta) Xinxin Wang (H3C) Ash Liao (Wiwynn) Nick Wang (Wiwynn)	Initial Release	0.5	03/03/2023
Song Kok Hang (AMD) Ahmed AbouAlfotouh (AMD) Xinxin Wang (H3C) Hongzheng Cai (H3C) Hao Zhang (H3C) Ash Liao (Wiwynn) Nick Wang (Wiwynn)	Added 7-Port x16 FC Topology Rotated OAM orientation on 8-Port Switch topology Fixed Section and Figure number	1.0	09/14/2023