UfiSpace Distributed Disaggregated Chassis (DDC) Routing System

S9705-48D Fabric White Box Specification

Revision 1.0

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2 Revision History

Date	Rev	Author	Summary of Change
Jan. 20, 2020	R1.0	Eric Wang	First Draft Release

3 Overview

This document describes the technical specifications of the S9705-48D designed for Distributed Disaggregated Chassis (DDC) Routing System for telco service application.

The S9705-48D is the best of breed robust, flexible and carrier-grade Distributed Disaggregated Chassis (DDC) fabric white box router that can be deployed in the core or edge to transport services over a scalable next-gen service provider network. Equipped with 400GE fabric ports, the S9705-48D enables fault and performance monitoring, non-stop routing support for control and data plane, and comprehensive high-availability networks.

The S9705-48D fabric couples with the S9700-53DX/23D line card white box routers in small, medium, and large clusters enabling 4Tb to 192Tb switching capacity. By connecting to the S9700-53DX/23D, it scales out not only economically and rapidly, but it also brings down the total cost of ownership.

The DDC Routing System adopts the innovated discrete Network Cloud Processor (NCP or line card white box) and Network Cloud Fabric (S9705-48D or fabric white box) building blocks providing flexibility to core router needs in the industry, integral to Ethernet switching performance and intelligence to networks while minimizing the network complexity.

Front View

Rear View

4 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9705-48D DDC white box router.

4.1 Feature Summary

- Ethernet I/O ports:
  - 48 x 400GE QSFPDD ports
- Front panel System / Port LED indicators:
  - 1 x System status LED
  - 1 x FAN status LED
  - 2 x PSU status LED
  - 48 x Port status LED
- Real panel LED indicators:
  - 1 x FAN status LED / Per Fan module (Total 4pcs)
  - 1 x PSU status LED / Per PSU (Total 2pcs)
- Management interfaces:
  - 1 x GE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact switch for system reset/reload default configuration

4.2 Component Summary

- PCBA:
  - 1 x Lower Switch Mainboard
  - 1 x Upper Switch Mainboard
  - 1 x CPU board
  - 1 x BMC module
  - 1 x FAN board
  - 1 x PSU adaptor board
  - 1 x Micro-USB board
- Onboard key components:
  - Top Switch Board
    - 1 x MAC Ramon Broadcom BCM88790
    - 6 x 56G PAM-4 re-timer BCM81358
  - Bottom Switch Board
    - 1 x MAC Ramon Broadcom BCM88790
    - 6 x 56G PAM-4 re-timer BCM81358
    - 1 x PCIe switch Broadcom PEX8724
    - 1 x BMC AST2400
    - 1 x PCIe NIC controller I210-IT for CPU
  - CPU board
    - 1 x CPU Broadwell-DE D-1548 with 8-core @ 2.0GHz
    - Up to 4 x 32GB DDR4 RDIMM memory module with ECC support
    - Up to 2 x 128GB SATA3 M.2 SSD Memory module
- PSU& FAN:
  - 1+1 2000W slim PSUs with redundancy support
  - 3+1 8038 FAN tray modules with redundancy support

4.3 Switch Board Functional Block Diagram

The S9705-48D system functional block diagram is shown as below:

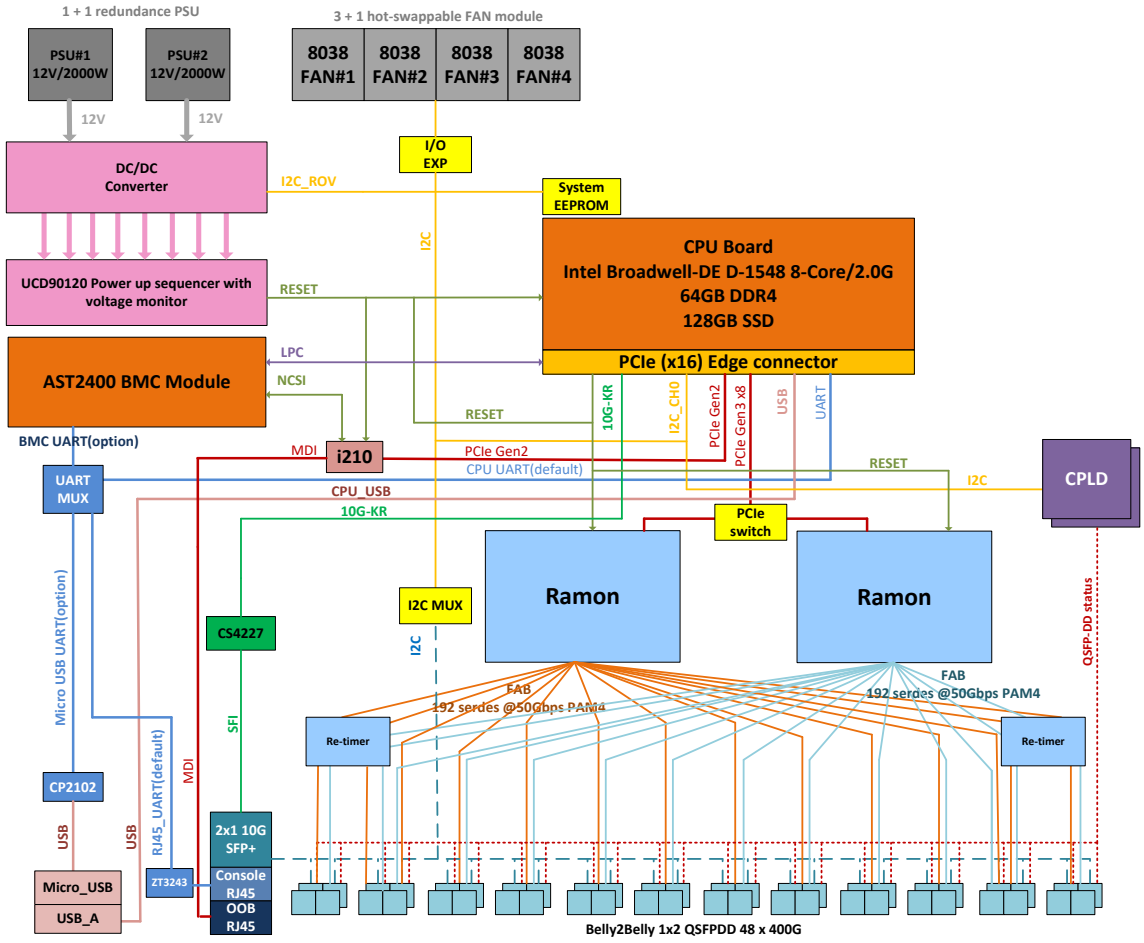


Figure 4-1 S9705-48D System Block Diagram

S9705-48D router main board placement is shown as below.

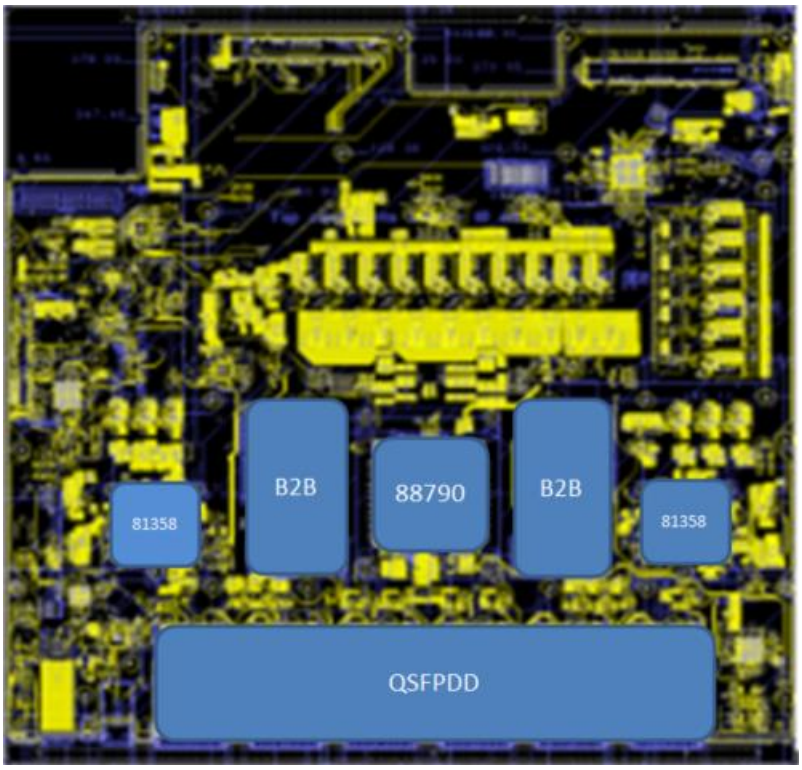


Figure 4-2 Bottom Main Board PCB Layout

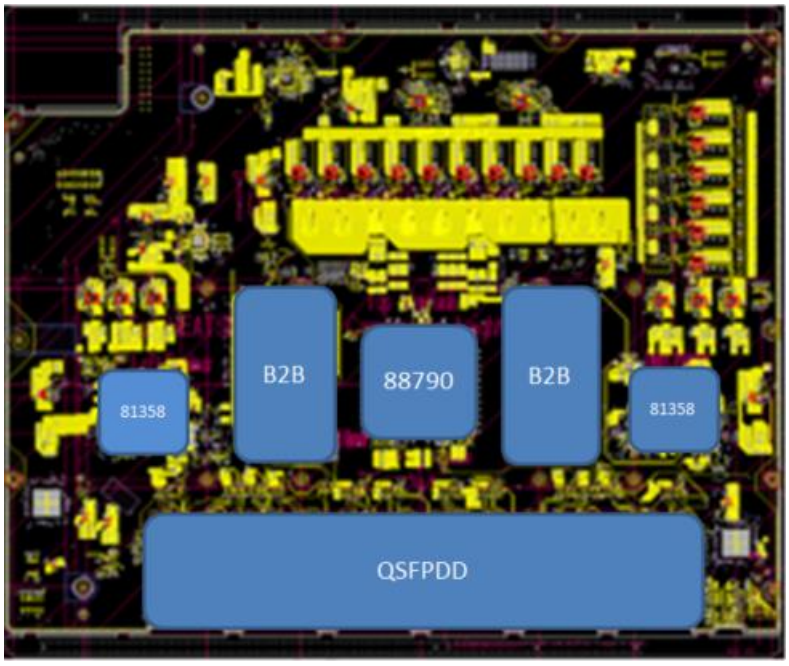


Figure 4-3 Top Main Board PCB Layout

4.4 CPU Board Functional Block Diagram

S9705-48D CPU board block diagram is shown as below:

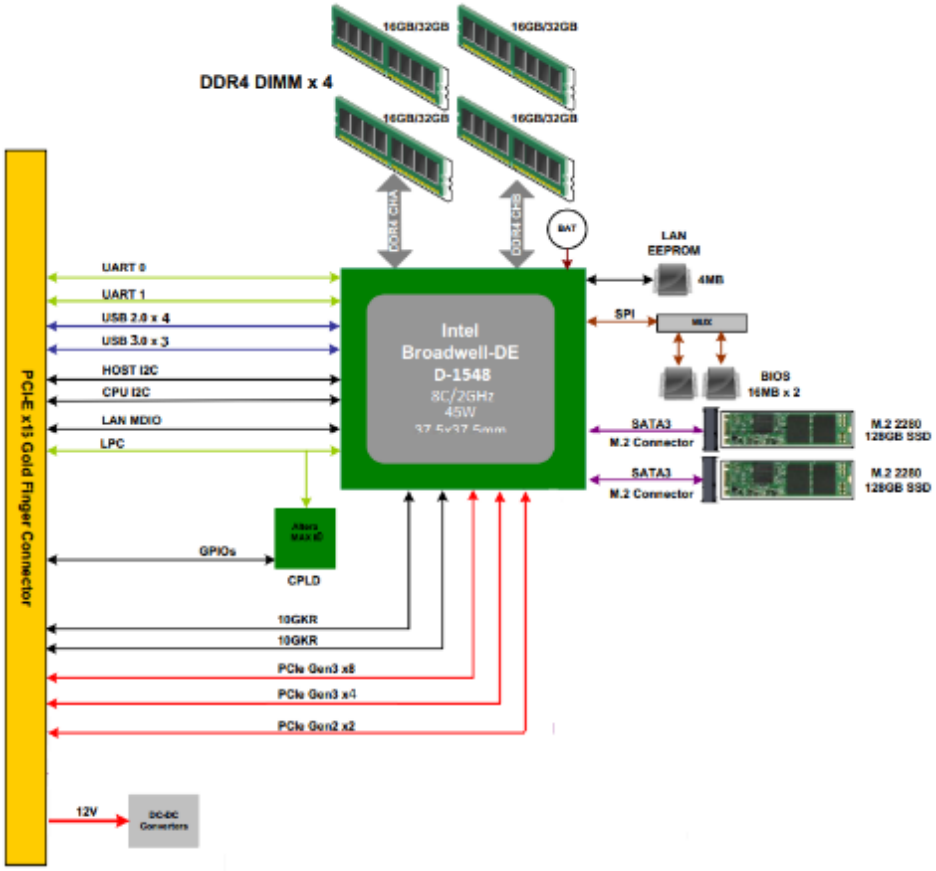


Figure 4-4 CPU Board Block Diagram

CPU board placement is shown as below:

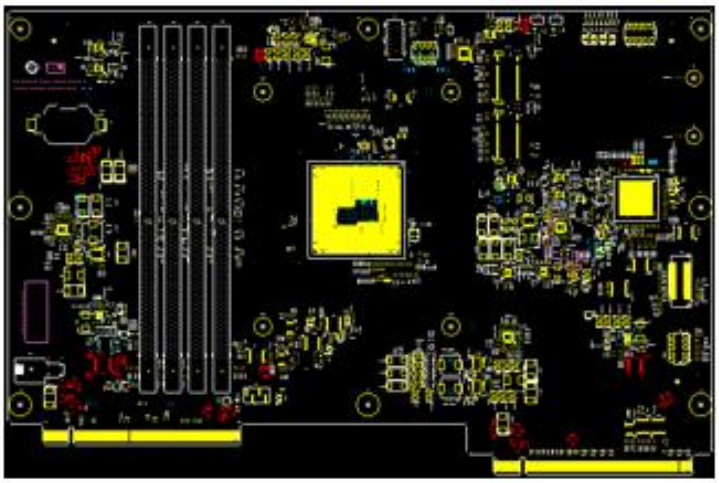


Figure 4-5 CPU Board PCB Layout

4.5 Mechanical Outline

S9705-48D chassis is designed to meet cabinet with 19'' depth installation requirement. This 2RU system mechanical dimension is: .436mmx762mmx87.7mm (WxDxH).

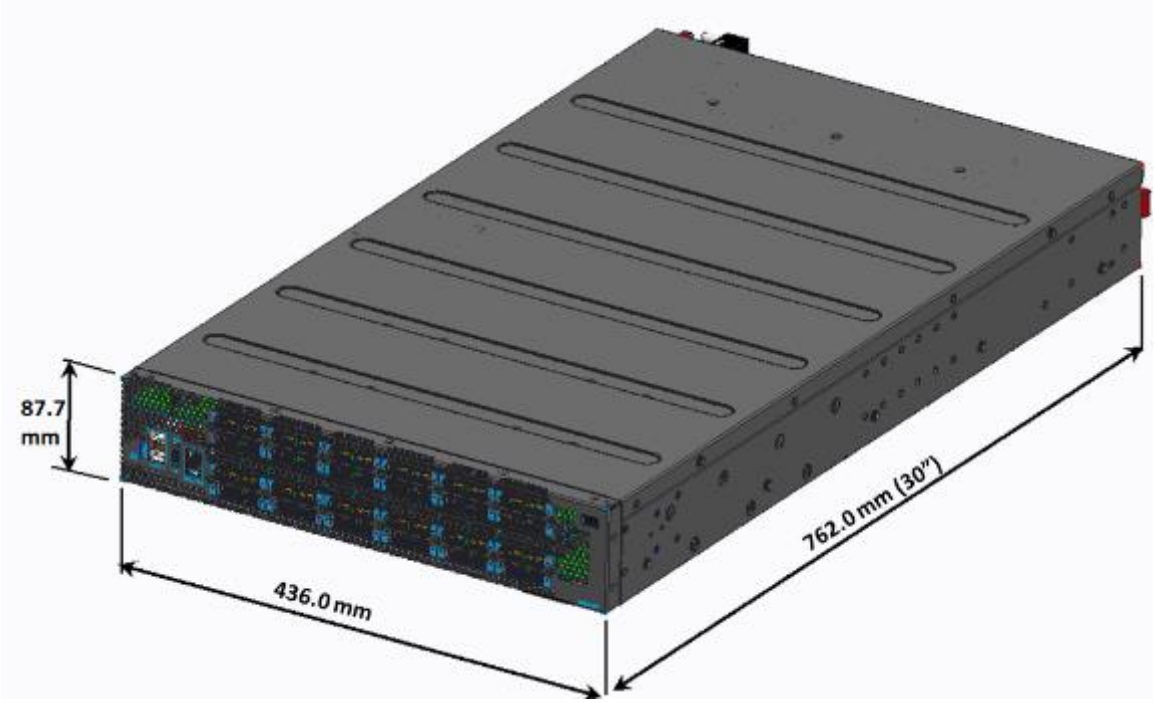


Figure 4-6 S9705-48D Mechanical Outline

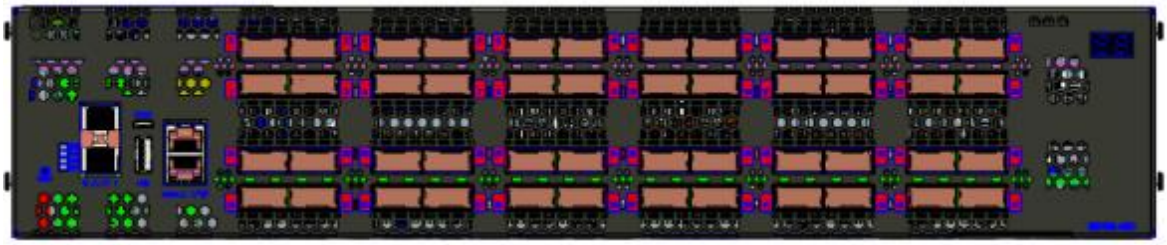


Figure 4-7 S9705-48D Front View

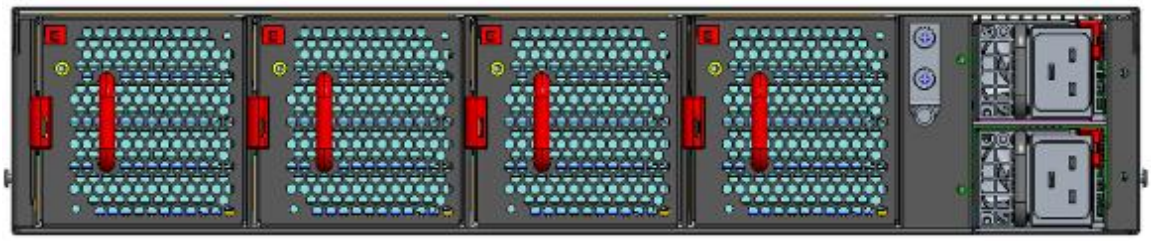


Figure 4-8 S9705-48D Rear View

S9705-48D system top view without top cover is shown as below :

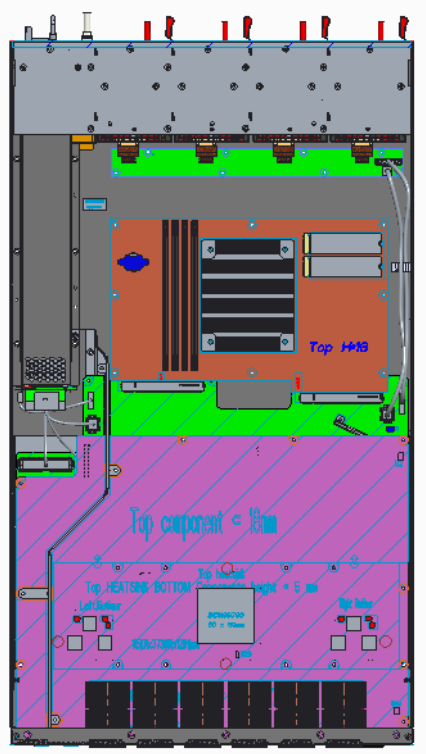


Figure 4-9 S9705-48D System Top View

5 Hardware Architecture

This section will focus on the detailed description of each major component used on the S9705-48D Fabric Element Router.

5.1 CPU Subsystem

Intel's x86 embedded SoC processor Broadwell-DE D-1548 is equipped on S9705-48D CPU board. The major onboard components and interfaces to switchboard are listed as below:

- Intel's Broadwell-DE Processor
  - ✓ Capable of supporting up to a 16-core processor
  - ✓ Four DDR4 ECC RDIMMs, up to 128GB
  - ✓ Two M.2 22*80mm SSD module up to 256GB
  - ✓ Dual 16MB SPI boot/BIOS flash components
- Two PCIe gold fingers to the switchboard
  - ✓ Single x8 PCIe Gen3 interface
  - ✓ Single x4 PCIe Gen3 interface
  - ✓ Single x2 PCIe Gen2 interface
  - ✓ Single SATA Gen3 interface
  - ✓ Two 10GKR Ethernet interfaces
  - ✓ Two UART interfaces
  - ✓ Three USB3 interfaces
  - ✓ Single LAN MDC/MDIO interface
  - ✓ Two SM_Bus interfaces

5.1.1 CPU Broadwell-DE

The key features of processor D-1500 product family are shown as below:

- The max base frequency running at 2.2GHz.
- 3 levels caching for the processor
  - ✓ Instruction Cache Unit (ICU) and Data Cache Unit (DCU): 32 KB each (64 KB total)
  - ✓ Mid-Level Cache (MLC) per core: 256 KB (instructions and data)
  - ✓ Last Level Cache (LLC) per socket: Up to 1.5 MB per Cbo (instructions and data)
- Two channels Integrated Memory Controller (IMC) for DDR3/DDR4 DIMMs
  - ✓ Supports 2 Gb and 4 Gb DRAM technologies with DDR3 (DDR3L only at 1.35V)
  - ✓ Supports 4 Gb and 8 Gb DRAM technologies with DDR4
- The Integrated I/O module provides PCIe interface
  - ✓ PCIe Gen3 speeds at 8 GT/s (no 8b/10b encoding)
  - ✓ X16 interface bifurcated down to two x8 or four x4 (or combinations)
  - ✓ X8 interface bifurcated down to two x4
- Two Integrated 10 GbE Controllers (MAC)
  - ✓ KX4 PHY supports:
    - – XAUI for XGMII extension (clause 47 of 802.3)
    - – 10GBASE-KX4 for gigabit backplane applications (IEEE802.3 clause 71)
    - – 2500BASE-KX for gigabit backplane applications
    - – 1000BASE-KX for gigabit backplane applications (IEEE802.3 clause 70)
  - ✓ KR PHY supports:
    - – 10GBASE-KR for gigabit backplane applications (IEEE802.3 clause 72)
    - – 1000BASE-KX for gigabit backplane applications (IEEE802.3 clause 70)
    - – 10GBASE SFP+ through a XFI compatible interface
    - – 10GBASE-T through a XFI compatible interface
- The Integrated PCH Logic provides extensive I/O support.
  - ✓ Eight ports PCIe GEN2 speeds up to 5 GT/s
  - ✓ ACPI Power Management Logic Support, Revision 4.0a
  - ✓ Enhanced DMA controller, interrupt controller, and timer functions
  - ✓ Integrated SATA host controllers with independent DMA operation on up to six ports
  - ✓ xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
  - ✓ One legacy EHCI USB controller provides a USB debug port.
  - ✓ Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
  - ✓ Version 2.0 SMBus with additional support for I2C devices
  - ✓ Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
  - ✓ Supports Intel® Trusted Execution Technology (Intel® TXT)
  - ✓ Integrated Clock Controller
  - ✓ Low Pin Count (LPC) interface
  - ✓ Firmware Hub (FWH) interface support
  - ✓ Serial Peripheral Interface (SPI) support
  - ✓ JTAG Boundary Scan support

5.1.2 DDR4 RDIMM

Four DDR4 RDIMM slots are designed in, up to 2400 MT/s are supported with both DIMMs populated. 8GB, 16GB and 32GB single rank (“1R”) and dual rank (“2R”), Note that CRC is not supported for DDR4.

The figure below shows the DDR4 interface connection between the CPU integrated memory controller and R-DIMM modules. Two 16GB R-DIMM modules are populated on S9705-48D CPU board by default.

5.1.3 SPI Boot Flash

There are two SPI boot flashes for Broadwell-DE BIOS storage. In manufacture, both of these two components store the same BIOS image. By default, system boots from primary SPI flash (#0). It will swap to backup SPI flash (#1) when system boot up fails from primary flash.

Dual boot flash design is also useful for system BIOS upgrade, in the case of the flash is crash during firmware upgrade, it will be recovered by the original image stored in the backup flash.

These two BIOS flashes are connected to the same SPI bus with two dedicated chip select (CS#) signals, see figure below for SPI connection.

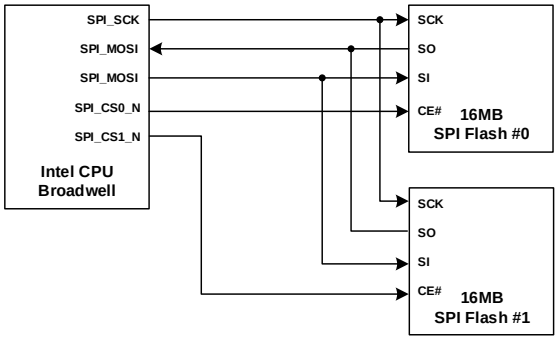


Figure 5-1 Intel Broadwell-DE BIOS Flash Connection

5.1.4 SATA M.2 SSD

The Broadwell-DE SoC contains Gen3 serial ATA ports capable of independent DMA operation. The SATA controllers are completely software transparent with an IDE Interface. Two M.2 connectors withM.2 22*80mm 128GBSSD are populated on CPU board.

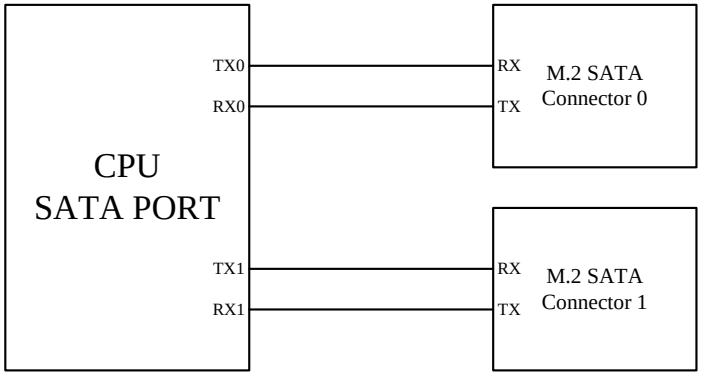


Figure 5-2 Intel Broadwell-DE SATA SSD Connection

5.1.5 USB

The SoC supports up to 4 USB 3.0 cable ports to provide support for SuperSpeed USB devices. In addition, the SoC supports up to 4 USB 2.0 ports that can be used to connect to high-speed, full-speed and low-speed USB devices. The SoC incorporates an XHCI controller and another EHCI controller. The four USB 3.0 ports are mapped to 4 of the existing USB 2.0 ports in the controller. USB 2.0 allows data transfers up to 480 Mb/s, and USB 3.0 up to 5 Gb/s. All USB interfaces are connected to PCIe golden finger.

USB Controller	Port Number	Net Name	Function description
PCI Device 29 Function 0(TBD)	1	USB2_PCH_P0_DN USB2_PCH_P0_DP	USB 2.0
	2	USB2_PCH_P1_DN USB2_PCH_P1_DP	USB 2.0
	3	USB2_PCH_P2_DN USB2_PCH_P2_DP	USB 2.0
PCI Device 20 Function 0(TBD)	1	USB3_RX_P0_N USB3_RX_P0_P USB3_TX_P0_N USB3_TX_P0_P	USB 3.0
	2	USB3_RX_P1_N USB3_RX_P1_P USB3_TX_P1_N USB3_TX_P1_P	USB 3.0
	3	USB3_RX_P2_N USB3_RX_P2_P USB3_TX_P2_N USB3_TX_P2_P	USB 3.0

Table 5-1 Broadwell-DE USB connection

5.1.6 DC/DC Power

CPU board is sourced by 12V DC power, which is delivered from switchboard. All power rails for CPU, R-DIMM & SSD etc. components are converted by onboard DC/DC regulators. DC/DC power converter design is shown as below:

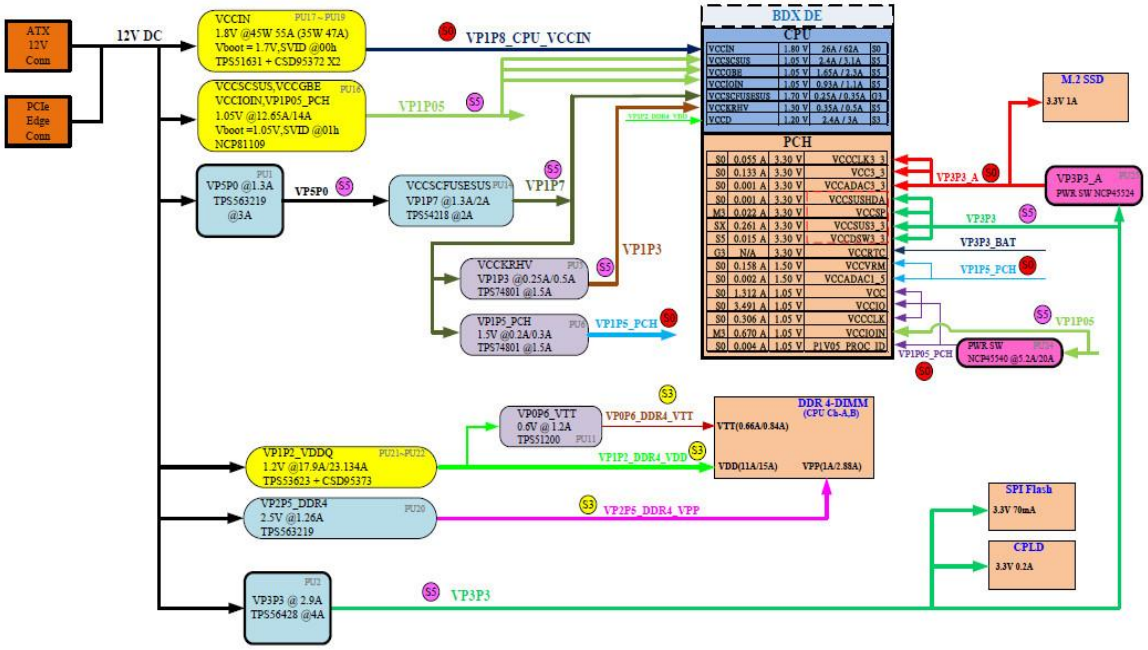


Figure 5-3 CPU board DC/DC Power Distribution Diagram

5.1.7 Clock Distribution

The integrated clock generator of Broadwell-DE provides 33MHz and 100MHz clock outputs to PCI and PCIe components, all other clocks for core, memory controllers, SDRAMs, SPI flash, and SMBus are also generated by internal clock controller. No external clock generator is needed.

Only two 25MHz XTALs and one 32.768KHz XTAL are populated on CPU board.

The figure below shows the CPU board clock distribution design.

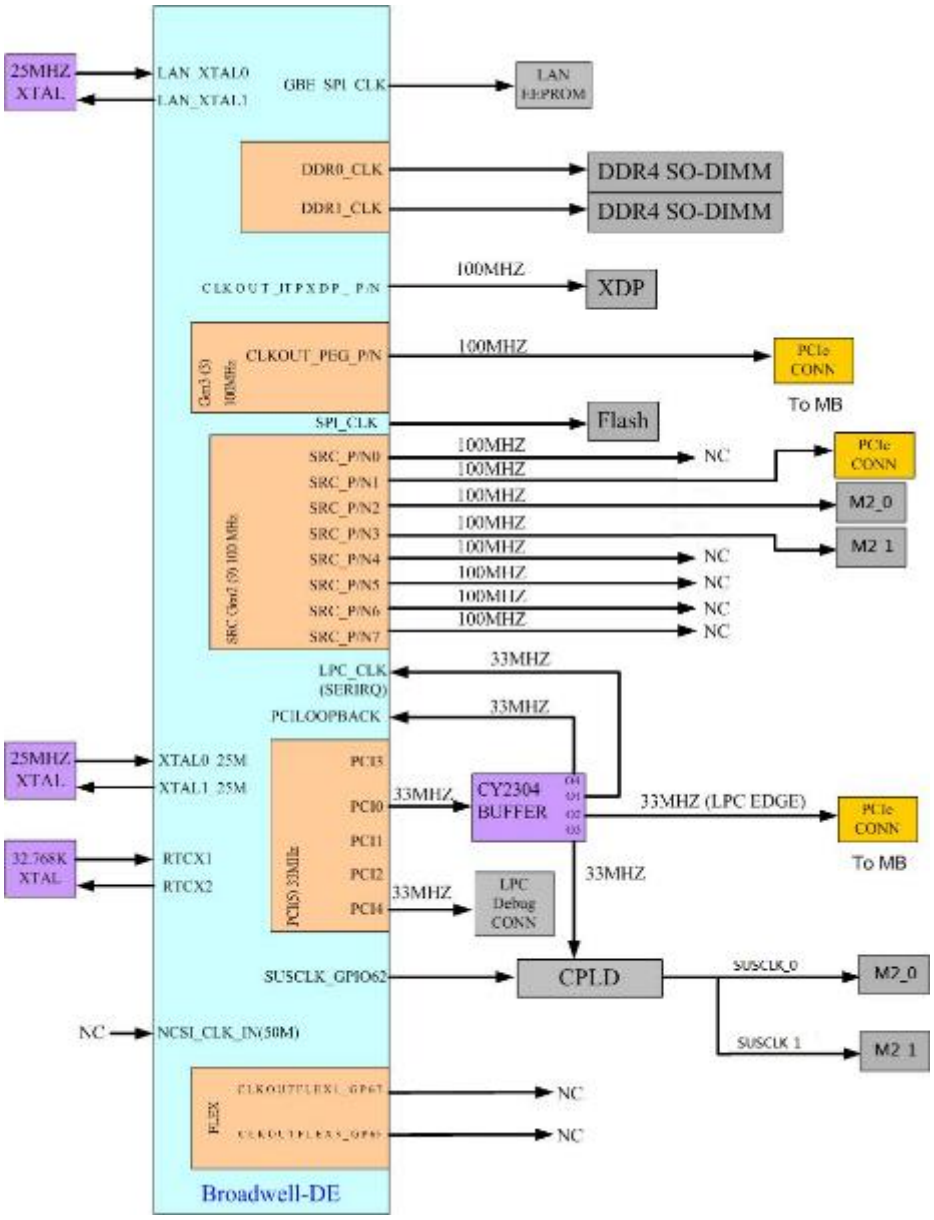


Figure 5-4 CPU board Clock Distribution Diagram

5.1.8 Reset Control

CPU reset is controlled by onboard CPLD, reset pin will be de-asserted once all DC/DC power rails are converted by expected. CPU can also be reset by tact switch button located on the left of front panel.

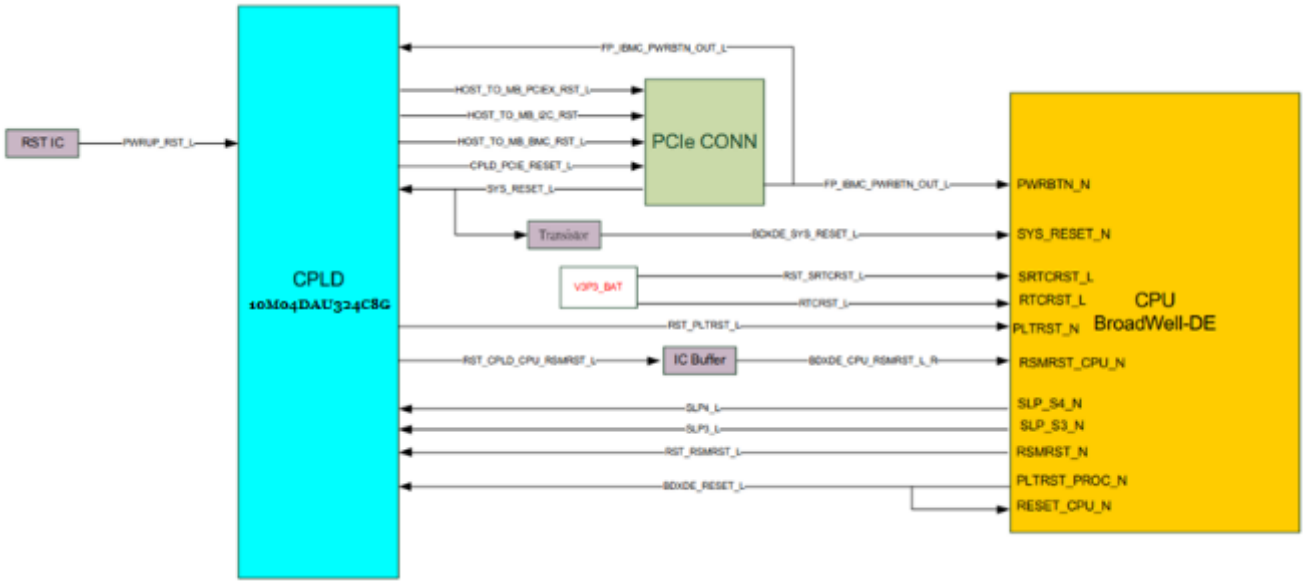


Figure 5-5 CPU board Reset Diagram

5.1.9 SMBus/I2C Interface

There are two SMBus/I2C interfaces for CPU board and switchboard components management.

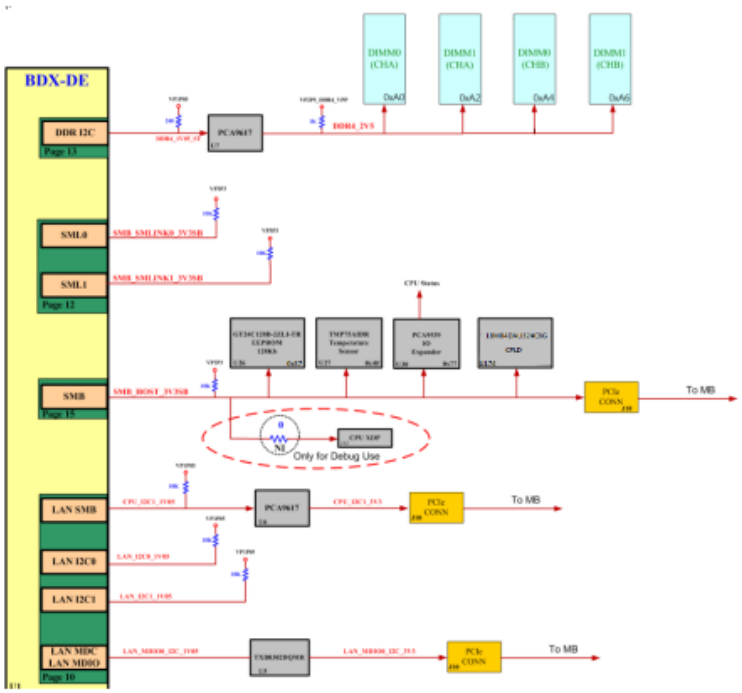


Figure 5-6 CPU board SMBus/I2C Interfaces Diagram

5.2 BMC Subsystem

In the S9705-48D, the baseboard management controller (BMC) autonomously monitors system's health including temperature, voltage, fan speed, etc. We use the DDR4 SO-DIMM connector as the BMC module connector. The BMC module connector is on the main board PCBA.

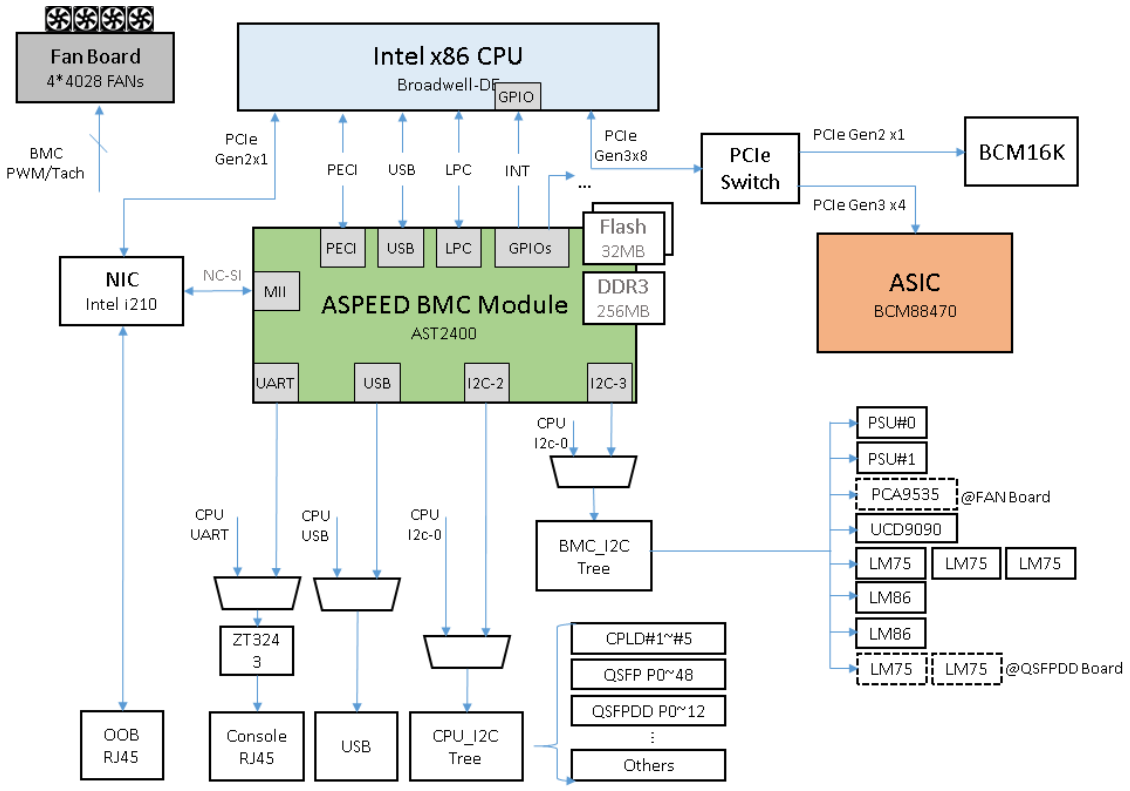


Figure 5-7 BMC Block Diagram

5.2.1 Key Interfaces and Configurations

5.2.1.1 LPC

Low-Pin-Count interface is an important interface for communication among Broadwell-DE, CPLD on CPU Board and BMC. The OS running in x86 use this interface to communicate with BMC's IPMI message handler.

5.2.1.2 USB

AST2400 provides three USB interfaces for different functional objectives. All USB controllers of AST2400 meet USB specification revision 2.0 and 1.1 and also compliant with EHCI and UHCI specification.

5.2.1.3 UART

AST2400 supports up to 5 sets UART IO interface with full flow control pins, and 1 set with Tx/Rx only for BMC console. The administrator can switch x86 and BMC console easily and choose to connect to front panel console RJ45 or micro-USB connector. Also, the BMC console could be disabled by command.

5.2.1.4 I2C

AST2400 integrates up to 14 sets of multi-function I2C/SMBus bus controllers used to collect voltage, temperature, FRU and manufacture information. The S9705-48D implements two I2C trees for management: CPU_I2C tree and BMC_I2C tree. Both two I2C trees could be accessed by CPU or BMC, but in default configuration, BMC only access the BMC_I2C tree. The CPLD on main switch board will take the arbitration

It monitors the system's health continuously after it boots up. BMC should record and handle the event when the sensor's values are out of reasonable range. Please refer to section 4.4.1 to get I2C device trees information for details.

5.2.1.5 PWM/Tacho

AST2400 integrates up to 8 sets of PWM outputs and 16 tachometer inputs. In the S9705-48D router, the BMC Implements 4 Fans in 3+1 redundancy.

5.3 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

5.3.1 Network Ports Design

This section describes the data path for each Ethernet fiber port and the management path for each PHY.

5.3.1.1 Network Port Path Configuration

This section shows the physical port location assignment and the Ethernet data path.

5.3.1.1.1 Physical Port Location Assignments

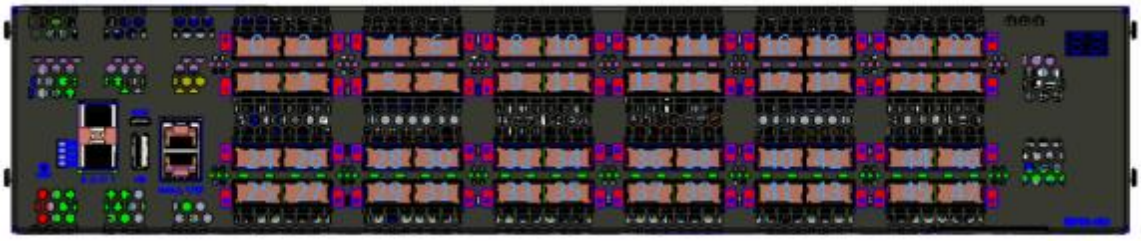


Figure 5-8 Physical Ports Assignment

5.3.2 DC/DC Power Design

Power distribution diagram is shown as below :

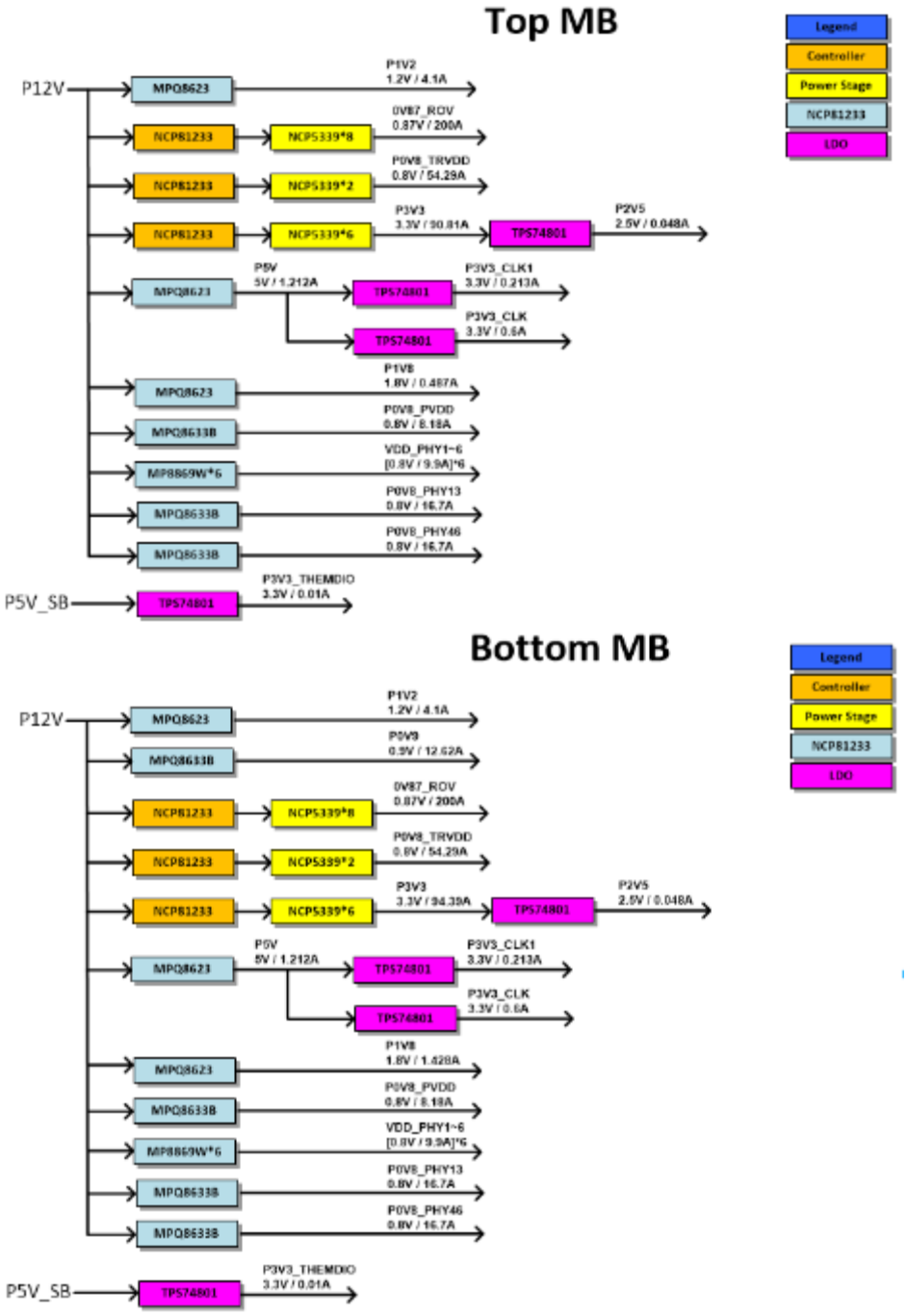


Figure 5-9 S9705-48D Top / Bottom MB Power Distribution

S9705-48D Top/Bottom main board clock diagram is shown as below:

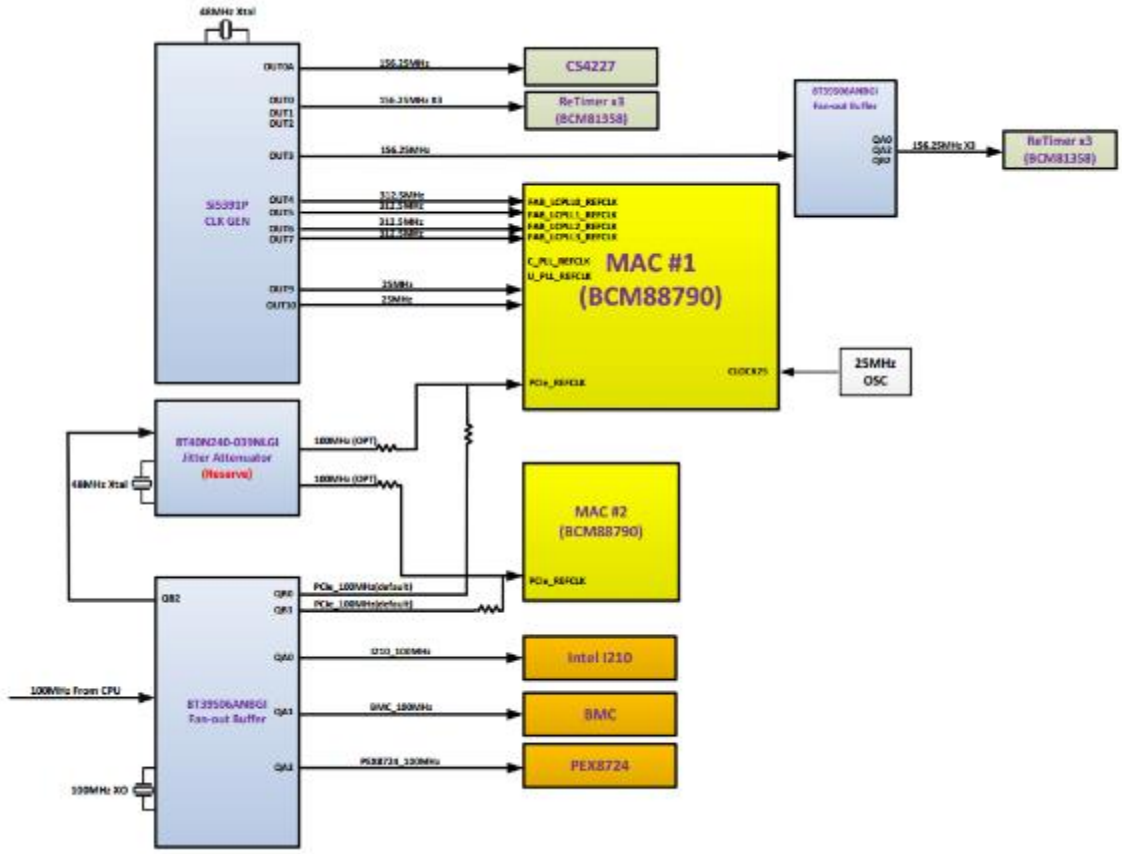


Figure 5-10 S9705-48D Switch Board Clock Diagram

5.4 System Management

5.4.1 System I²C Interface

There are two I2C buses on S9705-48D system, one is a CPU_I2C bus, and another one is BMC_I2C. Both CPU and BMC can access the buses but they need to negotiation to each other and always only one host can access the buses. The feature of these two buses:

- CPU_I2C: Access to I2C devices including CPLDs, I/O Ports, peripherals.
- BMC_I2C: Access to I2C devices including PSU, FAN, thermal sensors.

S9705-48D's system I2C block diagram is shown as below:

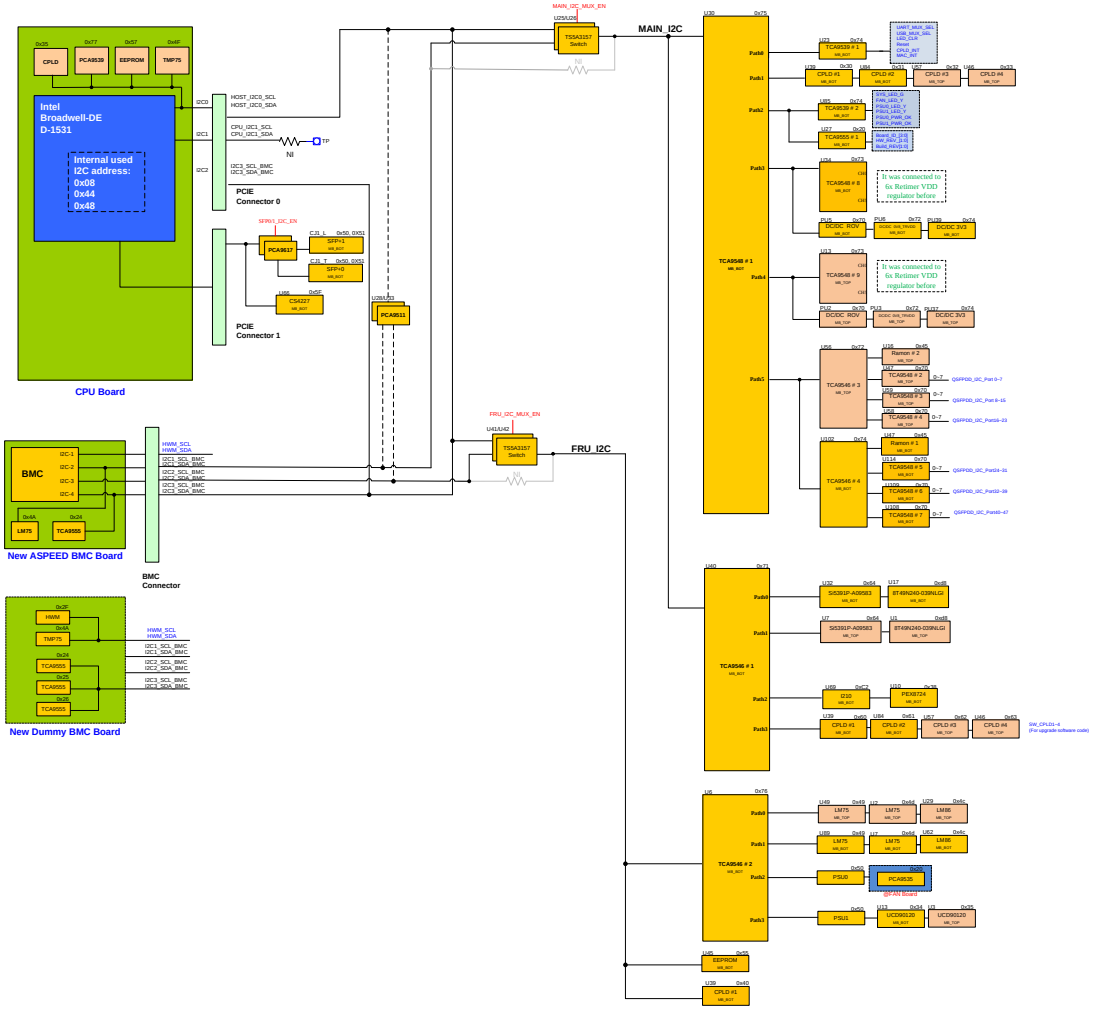


Figure 5-11 S9705-48D system I²C tree

CPU_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
CPU_I2C	EEPROM	101-0101	0x55	M24128	--	Main Board EEPROM
	I/O EXP	111-0000	0x70	TCA9539	0.7	IN_SEL1
					0.6	IN_SEL0
					0.5	UART_MUX_SEL
					0.4	USB_MUX_SEL
					0.3	HOST_TO_BMC_I2C_GPIO
					0.2	LED_CLR
					0.1	9539_PCIe_RST_N (Reserved)
					0.0	9539_MAC_RST_N (Reserved)
					1.7	I210_RST_L

I2C Bus	Name	Address		Device	Bit #	Function
					1.6	I210_PE_RST_L
					1.5	Si5391_INTR
					1.4	CPLD_TO_CPU_INT_L
					1.3	LM86_OT
					1.2	49N240_INTn
					1.1	PCIEX_INT#
					1.0	Ramon_TO_IO_INT_L
	I2C MUX	111-0101	0x75	TCA9548	--	CH0: IO expander for UART_MUX_SEL, LED_CLR...etc. CH1: CPLDs of top and bottom board. CH2: IO expander for system LED, board ID...etc. CH3: DC-DC controller of bottom board. CH4: DC-DC controller of top board. CH5: TCA9546 for two Ramon, QSFP-DD#1~48.
	I2C MUX	111-0010	0x72	TCA9548	--	QSFP28 Port 1~40 I2C QSFPDD Port 1 ~13 I2C
	I2C MUX	111-0011	0x73	TCA9548	--	TCA9548#8 Connection: CH0: VDD_PHY1 PWR controller. CH1: VDD_PHY2 PWR controller. CH2: VDD_PHY3 PWR controller. CH3: VDD_PHY4 PWR controller. CH4: VDD_PHY5 PWR controller. CH5: VDD_PHY6 PWR controller.
	Device				**Ch #**	**Function**
	TCA9548 0x71				Ch0	CPLD1~CPLD5 , 0x30 ~ 0x34
					Ch1	TCA9539, 0x75 Ch1.7: Unused Ch1.6: Unused Ch1.5: Unused Ch1.4: Unused Ch1.3: Unused Ch1.2: Unused Ch1.1: PSU0_PWROK Ch1.0: PSU1_PWROK Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: PSU0_LED_Y Ch0.3: PSU1_LED_Y Ch0.2: FAN_LED_Y Ch0.1: FAN_LED_EN Ch0.0: PSU0_LED_Y
					Ch2	TCA9555, 0x27 Ch1.7: Board_ID_3 Ch1.6: Board_ID_2 Ch1.5: Board_ID_1 Ch1.4: Board_ID_0

I2C Bus	Name	Address		Device	Bit #	Function
						Ch1.3: HW_REV_1 Ch1.2: HW_REV_0 Ch1.1: Build_REV_1 Ch1.0: Build_REV_0 Ch0.7: Unused Ch0.6: Unused Ch0.5: Unused Ch0.4: Unused Ch0.3: Unused Ch0.2: Unused Ch0.1: Unused Ch0.0: Unused
					Ch3	DC/DC ROV, 0x75
					Ch4	DC/DC AVS, 0x75
					Ch5	TCA9539, 0x75 Voltage High/Low margin test
					Ch6	Unused
					Ch7	Unused
	Device				**Ch #**	**Function**
	TCA9548 0x72				Ch0	TCA9548, 0x75 Ch0: QSFP28 Port 0 I2C Ch1: QSFP28 Port 1 I2C Ch2: QSFP28 Port 2 I2C Ch3: QSFP28 Port 3 I2C Ch4: QSFP28 Port 4 I2C Ch5: QSFP28 Port 5 I2C Ch6: QSFP28 Port 6 I2C Ch7: QSFP28 Port 7 I2C
					Ch1	TCA9548, 0x75 Ch0: QSFP28 Port 8 I2C Ch1: QSFP28 Port 9 I2C Ch2: QSFP28 Port 10 I2C Ch3: QSFP28 Port 11 I2C Ch4: QSFP28 Port 12 I2C Ch5: QSFP28 Port 13 I2C Ch6: QSFP28 Port 14 I2C Ch7: QSFP28 Port 15 I2C
					Ch2	TCA9548, 0x75 Ch0: QSFP28 Port 16 I2C Ch1: QSFP28 Port 17 I2C Ch2: QSFP28 Port 18 I2C Ch3: QSFP28 Port 19 I2C Ch4: QSFP28 Port 20 I2C Ch5: QSFP28 Port 21 I2C Ch6: QSFP28 Port 22 I2C Ch7: QSFP28 Port 23 I2C
					Ch3	TCA9548, 0x75 Ch0: QSFP28 Port 24 I2C Ch1: QSFP28 Port 25 I2C Ch2: QSFP28 Port 26 I2C

I2C Bus	Name	Address		Device	Bit #	Function
						Ch3: QSFP28 Port 27 I2C Ch4: QSFP28 Port 28 I2C Ch5: QSFP28 Port 29 I2C Ch6: QSFP28 Port 30 I2C Ch7: QSFP28 Port 31 I2C
					Ch4	TCA9548, 0x75 Ch0: QSFP28 Port 32 I2C Ch1: QSFP28 Port 33 I2C Ch2: QSFP28 Port 34 I2C Ch3: QSFP28 Port 35 I2C Ch4: QSFP28 Port 36 I2C Ch5: QSFP28 Port 37 I2C Ch6: QSFP28 Port 38 I2C Ch7: QSFP28 Port 39 I2C
					Ch5	TCA9548, 0x75 Ch0: Reserved for QSFP28 Port 40 I2C Ch1: Reserved for QSFP28 Port 41 I2C Ch2: Reserved for QSFP28 Port 42 I2C Ch3: Reserved for QSFP28 Port 43 I2C Ch4: Reserved for QSFP28 Port 44 I2C Ch5: Reserved for QSFP28 Port 45 I2C Ch6: Reserved for QSFP28 Port 46 I2C Ch7: Reserved for QSFP28 Port 47 I2C
					Ch6	TCA9548, 0x75 Ch0: QSFPDD Port 0 I2C Ch1: QSFPDD Port 1 I2C Ch2: QSFPDD Port 2 I2C Ch3: QSFPDD Port 3 I2C Ch4: QSFPDD Port 4 I2C Ch5: QSFPDD Port 5 I2C Ch6: QSFPDD Port 6 I2C Ch7: QSFPDD Port 7 I2C
					Ch7	TCA9548, 0x75 Ch0: QSFPDD Port 8 I2C Ch1: QSFPDD Port 9 I2C Ch2: QSFPDD Port 10 I2C Ch3: QSFPDD Port 11 I2C Ch4: QSFPDD Port 12 I2C Ch5: Reserved for QSFPDD 13 Ch6: Unused Ch7: Unused
	Device				**Ch #**	**Function**
	TCA9548 0x73				Ch0	SFP+1, 0x50, 0x51
					Ch1	SFP+0, 0x50, 0x51
					Ch2	CPLD1~CPLD5, 0x60~0x64 For CPLD firmware upgrade
					Ch3	Clock generators 82P33814ANLG, 0x53 8V19N474BFGI, 0x6C
					Ch4	10G dual PHY CS4227, 0x40
					Ch5	PCIE Switch PEX8724, 0x38
					Ch6	Ethernet Controller I210, 0xC2

I2C Bus	Name	Address		Device	Bit #	Function
					Ch7	Unused

BMC_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
FRU_I2C	I2C MUX	111-0100	0x74	TCA9548	--	FRU units, thermal sensors
	Device				**Ch #**	**Function**
	TCA9548 0x74				Ch0	PSU0, 0x50
					Ch1	PSU1, 0x50
					Ch2	PCA9535, 0x20 (at Fan board) Ch1.7: FAN4_DIR Ch1.6: FAN4_ABS Ch1.5: FAN4_LED_Y Ch1.4: FAN4_LED_G Ch1.3: FAN3_DIR Ch1.2: FAN3_ABS Ch1.1: FAN3_LED_Y Ch1.0: FAN3_LED_G Ch0.7: FAN2_DIR Ch0.6: FAN2_ABS Ch0.5: FAN2_LED_Y Ch0.4: FAN2_LED_G Ch0.3: FAN1_ABS Ch0.2: FAN1_ABS Ch0.1: FAN1_LED_Y Ch0.0: FAN1_LED_G
					Ch3	Voltage monitor UCD9090, 0x34 HWM W83795, 0x2F (Reserved for dummy BMC board)
					Ch4	Thermal sensor LM75, 0x49 Thermal sensor LM75, 0x4D Thermal sensor LM75, 0x4E
					Ch5	Thermal sensor LM86, 0x4C
					Ch6	Thermal sensor LM86, 0x4C
					Ch7	Thermal sensor LM75, 0x4D Thermal sensor LM75, 0x4E (at QSFPDD board) Thermal sensor TMP75, 0x4A (Reserved for dummy BMC board)

Table 5-2 IO Expander in I^2C Bus Description Table

5.4.2 System PCIe Interface

PCIe Gen 2, 3 interfaces are used to manage the slave devices by host CPU. PCIe slave component includes two Ramon BCM88790. There is one PCIe switch PEX8724 between host CPU and BCM88790 through PCIe Gen3 interface as below PCIe connection diagram.

PCIe interrupt from these components are wired together and connected to CPU board. CPU should scan PCIe devices one by one to check where the interrupt events come from.

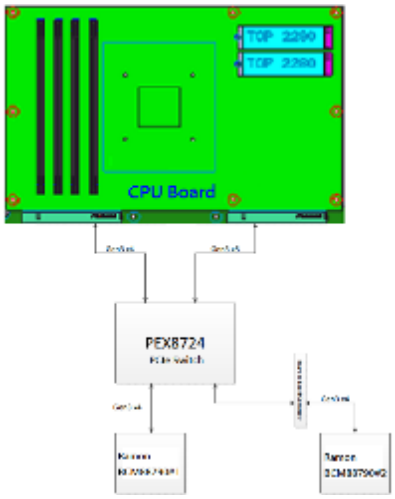


Figure 5-12 PCIe Connection Diagram

5.5 Other Daughter Boards

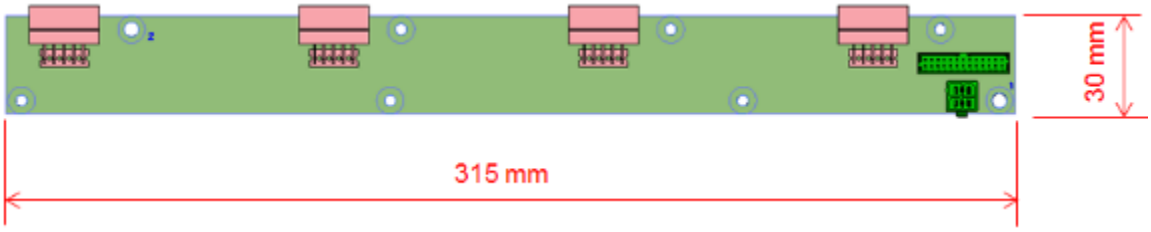
There are 3 daughter boards on the S9705-48D system. It includes FAN board, PSU Board, and OOB board. The description detial show as below.

5.5.1 FAN Board

The fan expander board is a passive board that bridges 12V power and control I/O to the Fan modules.

5.5.1.1 PCB Dimensions

S9705-48D FAN board PCB Dimension.



5.5.1.2 PCB Layout

The PCB layout shows as below.

Figure 5-13 FAN Board PCB Layout

5.5.1.3 Connector Pin Definition

The following table is the pin definition of connectors on the FAN board.

Pin	1	3	5	7	9	11	13	15	17	19	21	23	25
Description	FAN0_F_DET	Reserve	FAN1_F_DET	Reserve	FAN2_F_DET	FAN_STATUS_INT_L	FAN_BOARD_SCL	FAN_BOARD_SDA	P12V	P12V	P12V	P12V	P12V
Pin	2	4	6	8	10	12	14	16	18	20	22	24	26
Description	Reserve	FAN3_F_DET	Reserve	FAN0_1_PWM	FAN2_3_PWM	P3V3	GND	GND	GND	GND	GND	GND	P12V

Table 5-3 2x13 connector Pin Definition (mates with MB)

Pin	1	2	3	4	5
Description	GND	P12V	FAN_PWM	P12V	FAN_LED_G
Pin	6	7	8	9	10
Description	FAN_LED_Y	FAN_F_DET	GND	FAN_DIR#	FAN_ABS#

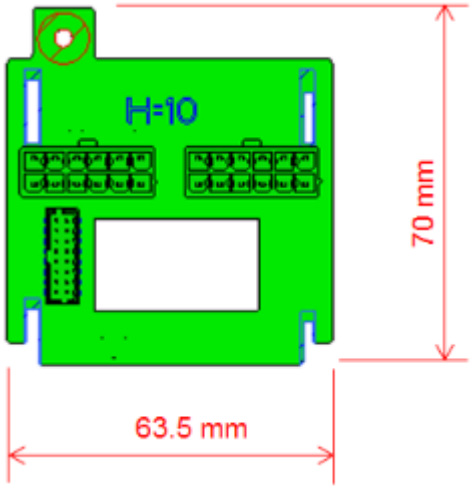
Table 5-4 2x5 connector Pin Definition (mates with FAN)

5.5.2 PSU Board

The PSU board is a passive board that bridges 12V power and control signals to the PSU.

5.5.2.1 PCB Dimensions

S9705-48D PSU board PCB Dimension.



5.5.2.2 PCB Layout

The PCB layout shows as below.

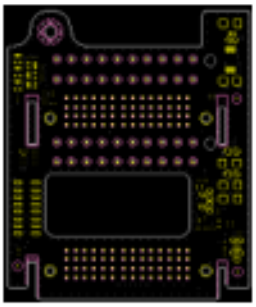


Figure 5-14 PSB Board PCB Layout

5.5.2.3 Connector Pin Definition

The following table is the pin definition of connectors on the PSB board.

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
A1	PSU_PRESENT	B1	PSU_PDB_FAULT	C1	GND	D1	P12V	P1_1	GND	P2_1	GND	P3_1	P12V	P4_1	P12V
A2	PSU_PDB_ALERT	B2	PSU_A0	C2	PSU_INT	D2	PSU_SHARE_PIN	P1_2	GND	P2_2	GND	P3_2	P12V	P4_2	P12V
A3	RESERVED	B3	AC_OK	C3	PSU_STATUS_SCL	D3	PSU_STATUS_SDA	P1_3	GND	P2_3	GND	P3_3	P12V	P4_3	P12V
A4	RESERVED	B4	RESERVED	C4	PSU_PWRON#	D4	GND	P1_4	GND	P2_4	GND	P3_4	P12V	P4_4	P12V
A5	RESERVED	B5	RESERVED	C5	PSU_A1	D5	PSU_PWROK								
A6	+5VSB	B6	+5VSB	C6	+5VSB	D6	+5VSB								

Table 5-5 Power Edge Connector Pin Definition (mates with PSU)

Pin	1	3	5	7	9	11	13	15
Description	PSU0_STATUS_SDA	PSU1_INT	PSU1_STATUS_SDA	PSU1_PRSNT	PSU1_PWROK	PSU1_PWRON	+5VSB	+5VSB
Pin	2	4	6	8	10	12	14	16
Description	PSU0_STATUS_SCL	PSU0_INT	PSU1_STATUS_SCL	PSU0_PRSNT	PSU0_PWROK	PSU0_PWRON	P3V3	GND

Table 5-6 2x8 signal connector Pin Definition (mates with MB)

Pin	1	3	5	7	9	11	13	15	17	19
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V
Pin	2	4	6	8	10	12	14	16	18	20
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V

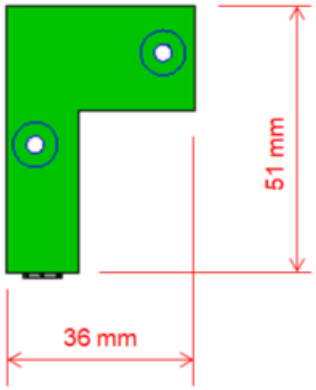
Table 5-7 Power connector Pin Definition (mates with MB)

5.5.3 Micro USB Board

The Micro USB board support USB to UART for Micro USB console port purpose.

5.5.3.1 PCB Dimensions

S9705-48D Micro USB PCB Dimension.



5.5.3.2 PCB Layout

The PCB layout shows as below.

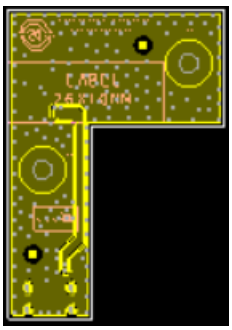


Figure 5-15 Micro USB Board PCB Layout

5.6 Front Panel Design

The S9705-48D front panel IO ports include below functionalities :

- System status LED
  - ✓ FAN status LED
  - ✓ PSU0 status LED
  - ✓ PSU1 status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ SFP+ ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB
- Ethernet data ports
  - ✓ 48x 400GE QSFPDD ports

Detailed IO arrangement is shown as below :

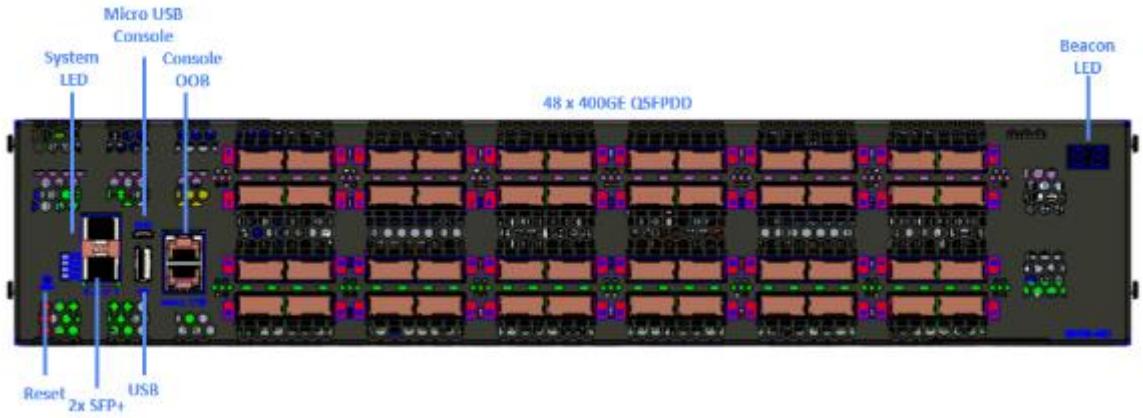


Figure 5-18 Front Panel IO Arrangement

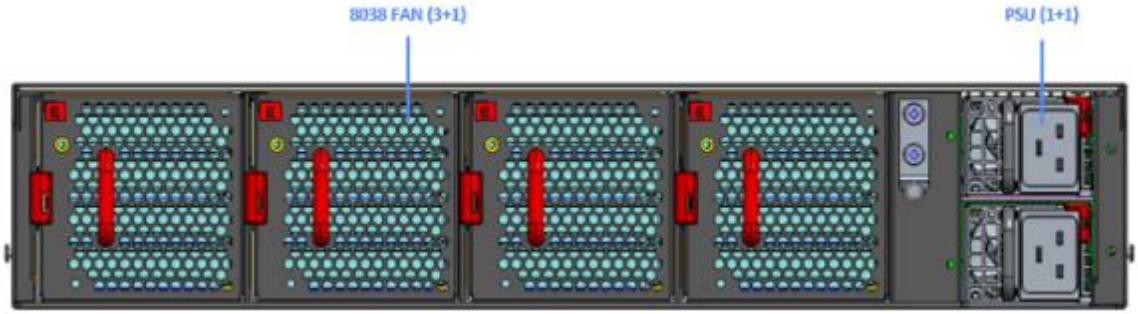


Figure 5-19 Rear Panel IO Arrangement

5.6.1 System LED Indicators

The system status and stacking LED are placed on main board and controlled by CPLD U39 address 0x30.

Items	LED Indication	Behavior	Description
1	SYS	OFF	No power
		Solid Green	Host CPU/BMC boot complete
		Solid Amber	Power is up but Host CPU/BMC boot failed
2	FAN	OFF	Fans are not initialized
		Solid Green	All Fans are work normal
		Solid Amber	Fan fail : one or more Fans need service
3	PS1	OFF	No power
		Solid Green	PSU1 is work normal
		Solid Amber	PSU1 fail (PSU1 need service)
4	PS2	OFF	No power
		Solid Green	PSU2 is work normal
		Solid Amber	PSU2 fail (PSU2 need service)

Table 5-12 System LED Descriptions

5.6.2 Management Port LED Indicators

The platform will have 2 green LEDs integrated in the front panel management RJ45 port.

Left LED:
- Off: no link
- Green-solid: Link-up

Right LED:
- Off: no activity
- Amber-blinking: TX/RX activity

5.6.3 SFP+ port LED Indicators

Each front panel SFP+ port will have one Green LED, and LED status is controlled by CPLD.

The following table shows the 1GE/10GE LED definitions:

Location	LED Indication	Color	Behavior	Description
E0 & E1 SFP+ ports	Link/Act/Speed of 10GE	Green	Solid	Link up
			Blinking	Packet transmitting or receiving
			Off	No link or port disable

Table 5-13 SFP+ port LED Descriptions

5.6.4 QSFPDD Port LED Indicators

CPLD will provide re-writeable port LED registers for BCM88790 port status indication. The SW function will keep polling the port status and then write the CPLD port LED register to control the LEDs of all QSFPDD ports.

Below figure shows the LED connection between CPLD and port LEDs.

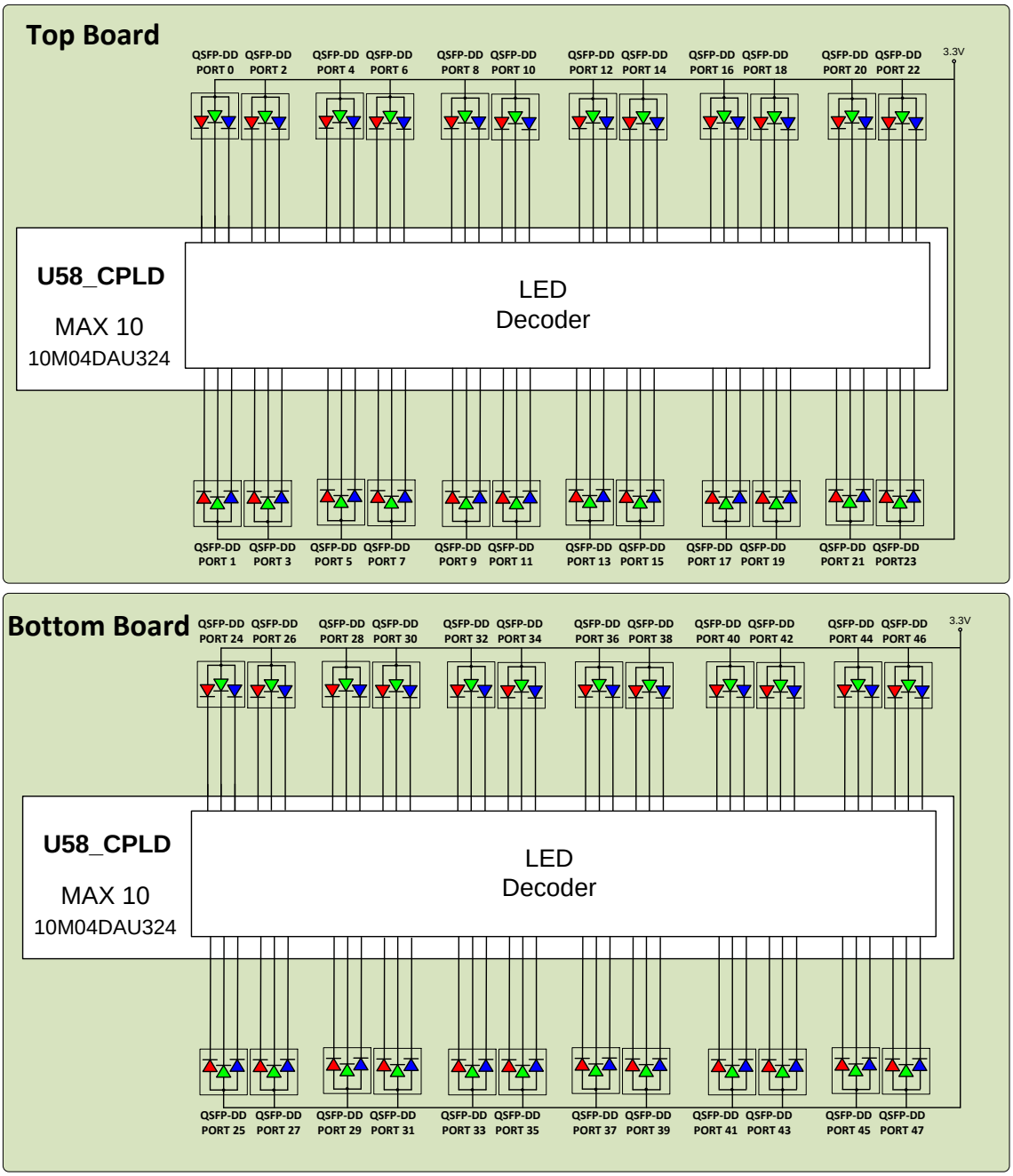


Figure 5-20 QSFPDD Port LEDs Control Diagram

5.6.5 OOB Port

The S9705-48D router includes 1 standard GE RJ45 port for out of band (OOB) management, share by CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

5.6.6 Console Port

Two console ports available for S9705-48D systems access, both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown as below. Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The default baud rate is 115200 bps.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

Table 5-14 Pin Definition of RJ45 Console Connector

5.6.7 USB2.0 Port

The S9705-48D router integrates a USB 2.0 host controller that supports a single port operating at high speed (HS) at 480 Mbps (USB 2.0).

USB 5V power will be enabled during system initialization, software should de-assert 'PWR_EN' by pulling this pin low once over current event (USB device consumes >0.5A current more than 20mS) is received. 'PWR_EN' need set as 'HIGH' to re-enable USB port.

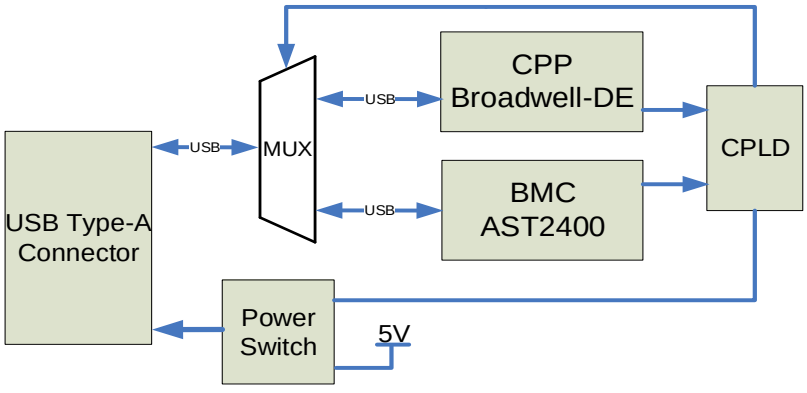


Figure 5-21 USB Interface Diagram

6 FAN Control and Thermal Policy

The FAN tray with 80x80x38mm FAN is adopted on the S9705-48D system to meet chassis depth requirement.

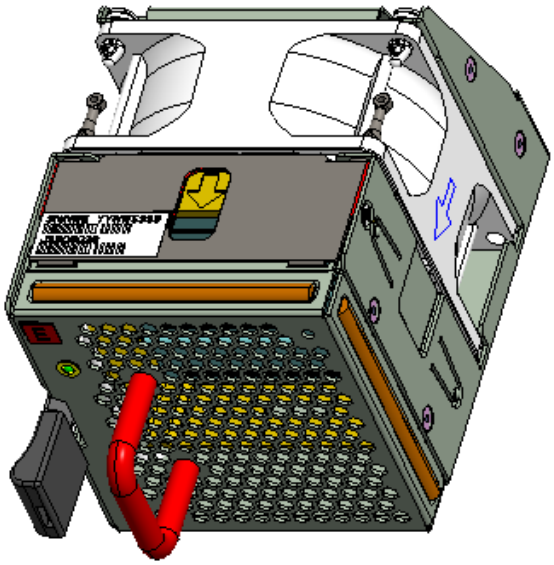


Figure 6-1 8038 FAN Module

6.1 Electrical Specifications

Rated voltage	12VDC
Rated current	3.5A MAX
Rated power consumption	48W MAX
Operating voltage range	10.8VDC ~ 13.2VDC
Operating temperature	-20 ~ +70
Rated speed	16100 +/- 1610 min-1
Acoustic noise	73dB MAX

7 Power Supply

The S9705-48D router adopts two kinds of 2000W hot swappable power supplies. The PSU modules are supported: One is 220Vac input to +12.2Vdc output AC/DC PSU, the other is -48Vdc input to +12.2Vdc output DC/DC PSU.

7.1 Physical Size

The physical size of the power supply enclosure is intended to accommodate the power range of up to 2000W. The physical size is 40mm x 50.5mm x 360mm (height x width x length).

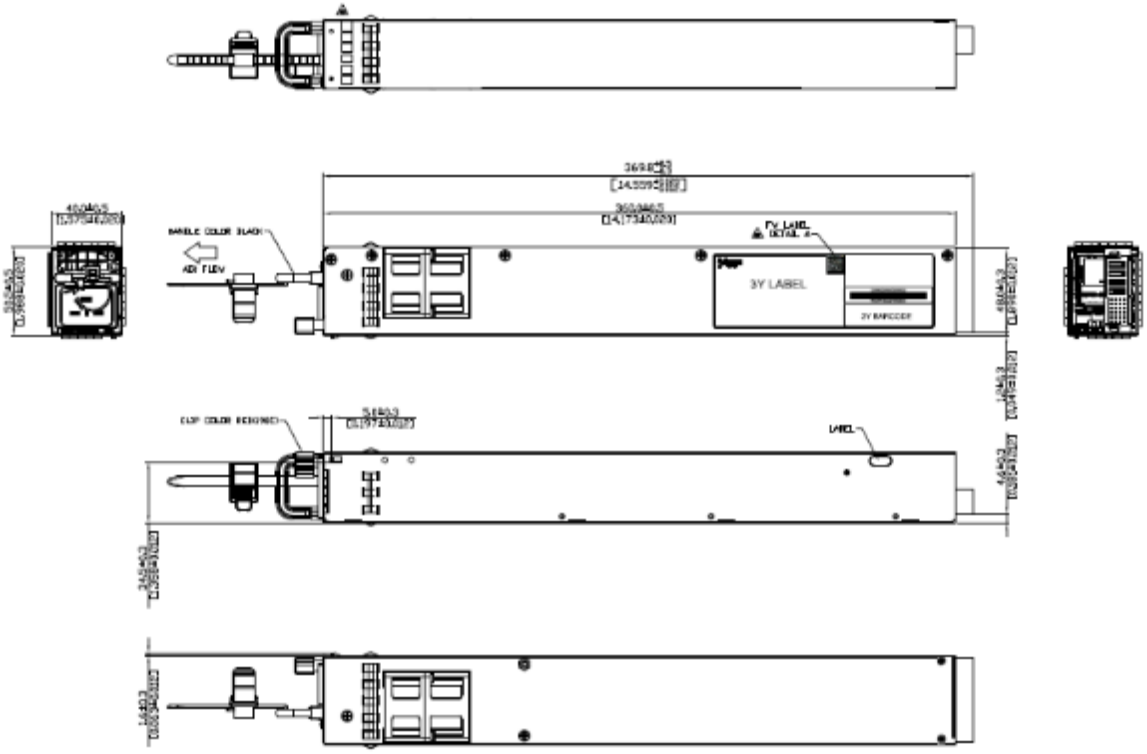


Figure 7-1 2000W AC/DC Power Supply Dimension

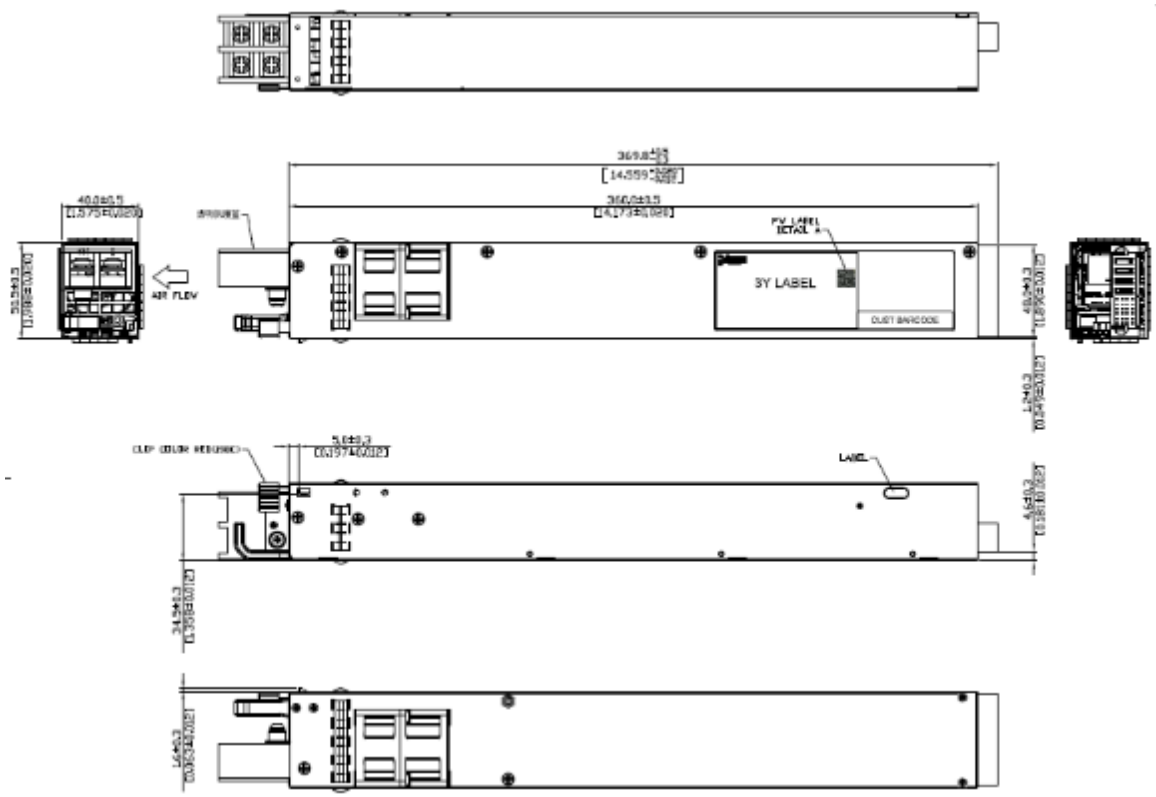


Figure 7-2 2000W DC/DC Power Supply Dimension

7.2 Electrical Specifications

Protection circuits inside the PSU shall cause only the main output to shutdown (latch off). If the PSU latches off due to a protection circuit assert, an Input power cycle off for 15sec or a PSON pin cycle high for 1sec shall be able to reset the PSU.

The detailed electrical specifications of AC/DC PSU are shown below:

INPUT SPECIFICATIONS	
Input Voltage Range	90~264Vac
Input Frequency	47-63 Hz
Input Current	13A max.
Inrush Current	100A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	90~264Vac:82A(+12.2V), 1000W 180~264Vac:164A(+12.2V), 2000W The output capacity varies depending on the input voltage, so for 2000W AC PSU the low-line 110Vac is disabled.
Max Power (Watt)	2000W@180~264Vac
Output Voltage (Volts)	+5VSB
Output Current (Amps)	5A (+5VSB)
Efficiency	80Plus Platinum >90% @20% load, >94 @50% load, >91% @100% load

Ripple P-P (mV) (max.)	+12.2V:200mV, +5VSB:50mV
Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	4msec
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1800Vac
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	Operating: 0 to 90% RH, Non-operating: 0 to 95% RH
EMI	Meets FCC part 15/CISPR 22 Class A(under 6dB)

Table 7-1 AC/DC Power Supply Specification

The detailed electrical specifications of DC/DC PSU are shown below:

INPUT SPECIFICATIONS	
Input Voltage Range	-40 ~ -72Vdc
Input Current	60A max.
Inrush Current	100A
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	164A(+12.2V), 2000W
Max Power (Watt)	2000W@-40~-72Vdc
STB Output Voltage (Volts)	+5VSB
STB Output Current (Amps)	5A (+5VSB)
Efficiency	>88% @20% load, >92 @50% load, >91% @100% load
Ripple P-P (mV) (max.)	+12.2V:120mV, +5VSB:50mV
Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	1msec
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1500Vdc
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	Operating: 0 to 90% RH, Non-operating: 0 to 95% RH
EMI	Meets FCC part 15/CISPR 22 Class A(under 6dB)

Table 7-2 DC/DC Power Supply Specification

Power supply condition	Power supply LED
Output ON and OK.	Green
No AC power to all power supplies.	Off
PSU standby state AC present / Only +5VSB on.	1Hz Flashing Green
AC cord unplugged or AC power lost with a second power supply in parallel still with AC input power.	1Hz Flashing Red
Power supply critical event causing a shutdown, failure, over current, short circuit, over voltage, fan failure, over temperature.	Red
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	Flashing 1sec Red and 1sec Green

Table 7-3 LED Status Information

Module	Module Pin Out	Dir.	BMC Pinout	Functionality Description
PSU #0	PSU0_PWROK	→	GPIOK7	PSU0 power OK signal generated by PSU
	PSU0_PRESENT_L	→	GPIOK6	PSU0 Slot. (0 : Present, 1 : Empty)
	PSU0_PSON_N	←	GPIOP2	PSU0 main power enable control by BMC
	PSU0_I2C	←	I2C2	PSU0 EEPROM access via I2C bus
	PSU0_INT_N	→	GPIOP3	PSU0 interrupt signal generated by PSU
PSU #1	PSU1_PWROK	→	GPIOP5	PSU1 power OK signal generated by PSU
	PSU1_PRESENT_L	→	GPIOP4	PSU1 Slot. (0 : Present, 1 : Empty)
	PSU1_PSON_N	←	GPIOE2	PSU1 main power enable control by BMC
	PSU1_I2C	←	I2C2	PSU1 EEPROM access via I2C bus
	PSU1_INT_N	→	GPIOP7	PSU1 interrupt signal generated by PSU

7.3 System Power Consumption

Power consumption of S9705-48D System :

TOP Main Board Power Consumption Estimation					ROV	PVDD0P8	TRVDD0P8		Retimer					CLK					
Item	Function/Part	Manufacturer	Mfg P/N	Qty	Voltage (V)													Power/Part	Total Power(W)	VR Efficiency	VR Input Current
					0.87	0.80	0.80	0.80	0.80	0.90	1.20	1.80	2.50	3.30	3.30	5.0	12.0				12V
1	FE	Broadcom	BCM88790	1	130	8.185	54.294				4.032	0.358			0.500			170.22	170.22	85%	16.69
2	Re-timer	Broadcom	BCM81358	6				9.904	5.577			0.081						12.53	75.18	85%	7.37
3	QSFP-DD	Standard		24											3.636			12.00	287.97	85%	28.23
4	CPLD	Altera	10M04DAU324C8GF	2							0.083		0.024		0.044			0.30	0.61	85%	0.06
5	CLK GEN	IDT	8V48NS0412	1										0.606				2.00	2.00	85%	0.20
6	100MHz CLK Buffer	IDT	8T39S06A	1										0.213				0.70	0.70	85%	0.07
7	OTHER(3.3V)	Standard		1											2.000			6.60	6.60	85%	0.65
8	LED	Standard		48											0.020			0.07	3.17	85%	0.31
9	P3V3_FAN	N/A	N/A	1											0.600			1.98	1.98	85%	0.19
10	P3V3_I2C	N/A	N/A	1											1.600			5.28	5.28	85%	0.52
	Total current(A)				130.000	8.185	54.294	59.424	33.462	0.000	4.198	0.844	0.048	0.819	93.012	0.000	0.000				53.57
	Total Payload Power (W) w/o DC/DC Losses				113.100	6.548	43.435	47.539	26.770	0.000	5.038	1.519	0.120	2.704	#######	0.000	0.000	553.71	546.45		
	D/D Efficiency				0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850				
	Each D/D input Power				133.059	7.704	51.100	55.928	31.494	0.000	5.927	1.787	0.141	3.181	#######	0.000	0.000				
	PSU Output Power Budget (W)																				651.43

Bottom Main Board Power Consumption Estimation					ROV	PVDD0P8	TRVDD0P8		Retimer					CLK					
Item	Function/Part	Manufacturer	Mfg P/N	Qty	Voltage (V)												Power/Part	Total Power(W)	VR Efficiency	VR Input Current
					0.87	0.80	0.80	0.80	0.80	0.90	1.20	1.80	2.50	3.30	3.30	5.0	12.0			12V
1	FE	Broadcom	BCM88790	1	130	8.185	54.294				4.032	0.358			0.500			170.22	170.22	85%	16.69
2	Re-timer	Broadcom	BCM81358	6				9.904	5.577			0.081						12.53	75.18	85%	7.37
3	QSFP-DD	Standard		24											3.636			12.00	287.97	85%	28.23
4	Ethernet Controller	Intel	I210	1											0.500			1.65	1.65	85%	0.16
5	Dual 15Gbps PHY	Inphi	CS4227	1						0.956		0.324						1.44	1.44	85%	0.14
6	PCIE switch	PEX	PEX8724-CA80BC G	1						11.67		0.260						10.97	10.97	85%	1.08
7	CPLD	Altera	10M04DAU324C8GF	2							0.083		0.024		0.044			0.30	0.61	85%	0.06
8	CLK GEN	IDT	8V48NS0412	1										0.606				2.00	2.00	85%	0.20
9	100MHz CLK Buffer	IDT	8T39S06A	1										0.213				0.70	0.70	85%	0.07
10	OTHER(3.3V)	Standard		1											2.000			6.60	6.60	85%	0.65
11	USB-TO-UART BRID	Silicon Labs	CP2104	1											0.500			1.65	1.65	85%	0.16
12	RS232 Transceivers	Zywyn	ZT3243	1											0.100			0.33	0.33	85%	0.03
13	LED	Standard		62											0.020			0.07	4.09	85%	0.40
14	USB (Type-A)			1												0.500		2.50	2.50	85%	0.25
15	USB (Micro_USB)			1												0.500		2.50	2.50	85%	0.25
16	P3V3_FAN	N/A	N/A	1											0.600			1.98	1.98	85%	0.19
17	P3V3_I2C	N/A	N/A	1											1.600			5.28	5.28	85%	0.52
	Total current(A)				130.000	8.185	54.294	59.424	33.462	12.626	4.198	1.428	0.048	0.819	94.392	1.000	0.000				56.44
	Total Payload Power (W) w/o DC/DC Losses				113.100	6.548	43.435	47.539	26.770	11.363	5.038	2.570	0.120	2.704	######	5.000	0.000	575.68	575.68		
	D/D Efficiency				0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850	0.850				
	Each D/D input Power				133.059	7.704	51.100	55.928	31.494	13.369	5.927	3.024	0.141	3.181	######	5.882	0.000				
	PSU Output Power Budget (W)																				677.27

Table 7-4 Power consumption of main board

Item	Sheet	Function / Subset	Qty	Power Consumption (W)
1	Top MB	Top Main Board	1	651
2	Bottom MB	Bottom Main Board	1	677
3	BMC	BMC module	1	14
4	CPU	CPU module	1	83
5	FAN	FAN module	4	168
Total Power consumption (W)				**1593.8**
PSU 12V total current(A)				132.8

Table 7-5 Power consumption of S9705-48D system

8 Software Support

The S9705-48D supports a base software package composed of the following components:

BIOS

The S9705-48D Supports AMI AptioV BIOS version xx or greater with the x86 CPU module

BMC

The S9705-48D Supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2400 platform.

ONIE

See http://onie.org/ for the latest supported version

9 Compliance

Environmental	
Operating temperature	0 ~ 45°C (at sea level with Fan Failure condition)
Storage temperature	-40~70°C (–40°F to 158°F)
Altitude	0~10,000ft at 45°C
Operating relative humidity	0%-85% RH (non-condensing)
Storage relative humidity	0%-85% RH (non-condensing)
Acoustic	76dB at 27°C
Dimensions (height x width x depth)	436.0 mm (W) x 762.0 mm (D) x 87.7 mm (H)
Weight	26.66kg

Regulatory Compliances	
Category	ATT-TP-76200 ESR-003 (Carrier Grade Level 3)
Safety	NEBS Level 3 UL 62368-1 IEC/EN 60950-1 IEC/EN 62368-1 BSMI CNS 14336-1 UL 60960
EMC	NEBS Level 3 FCC Part 15, Subpart B, Class A; EN55032, Class A EN 300 386 EN 55024 EN 301 489-1 EN 301 489-19 EN 303413 BSMI (CNS 13438), Class A