

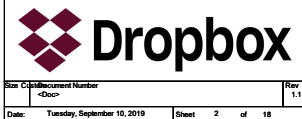
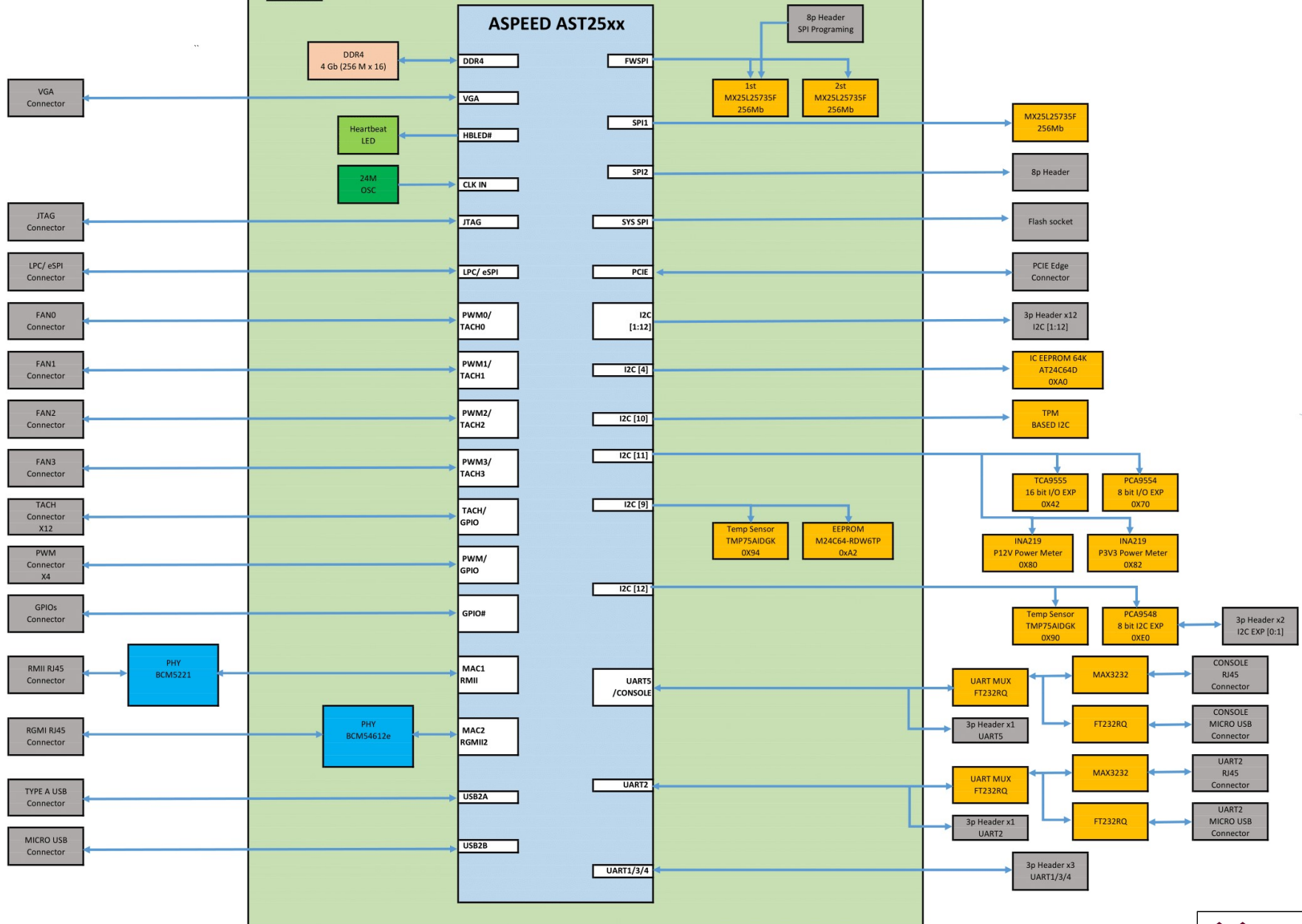
01	INDEX
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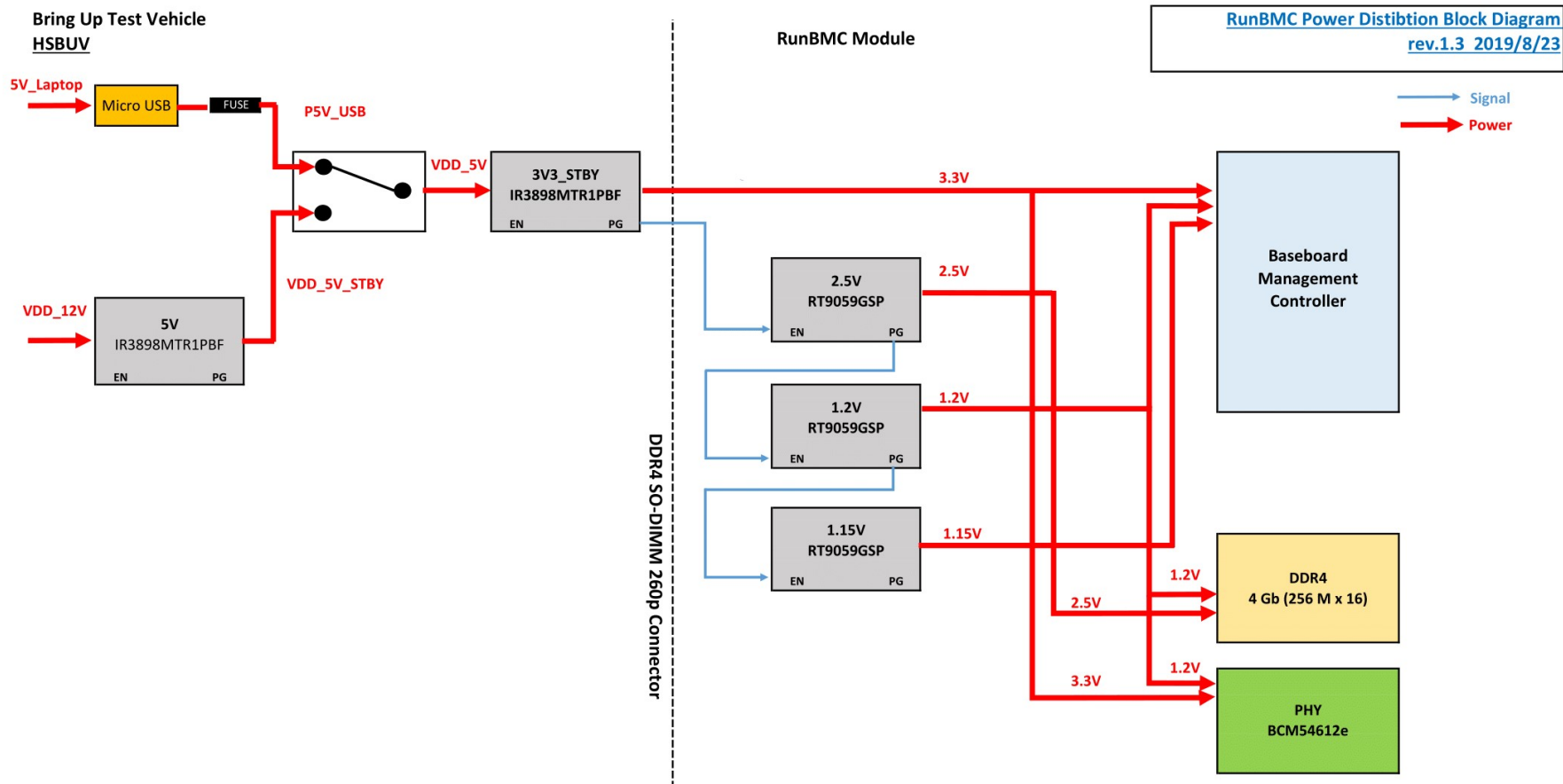
Bring Up Test Vehicle HSBUV

BMC Module HS2500

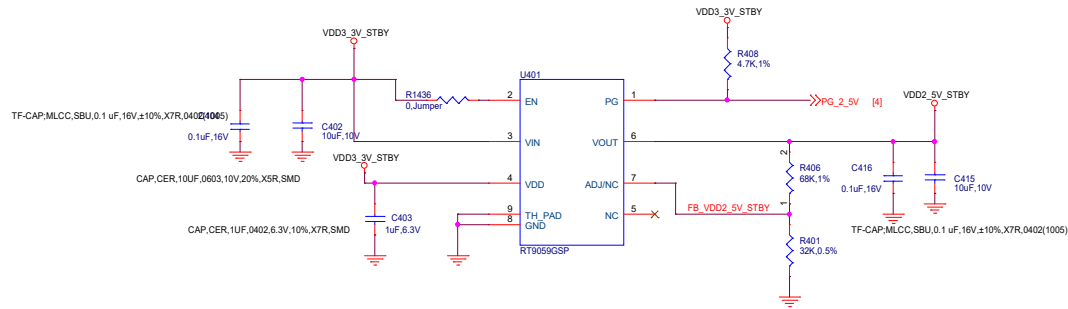
ASPEED AST25xx

RunBMC BMC Architecture Block Diagram
rev.1.3 10/09/2019



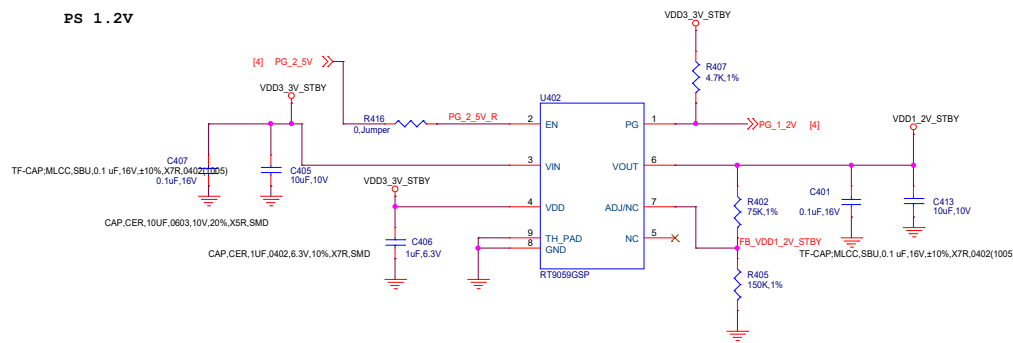


PS 2.5V

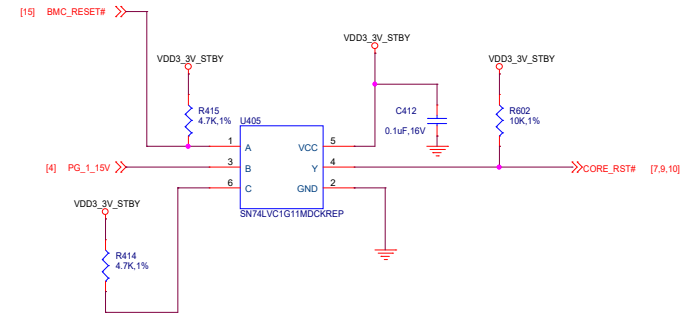
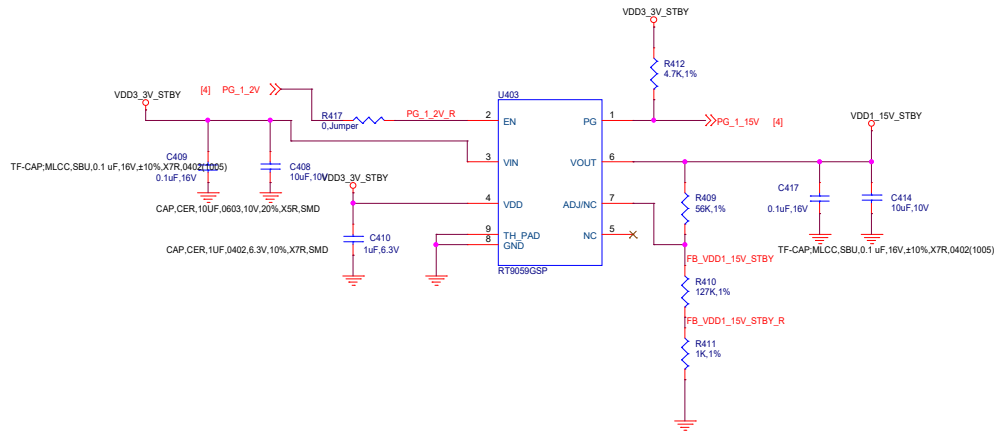


NOTE:
The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9059 and returned to a clean analog ground.

PS 1.2V



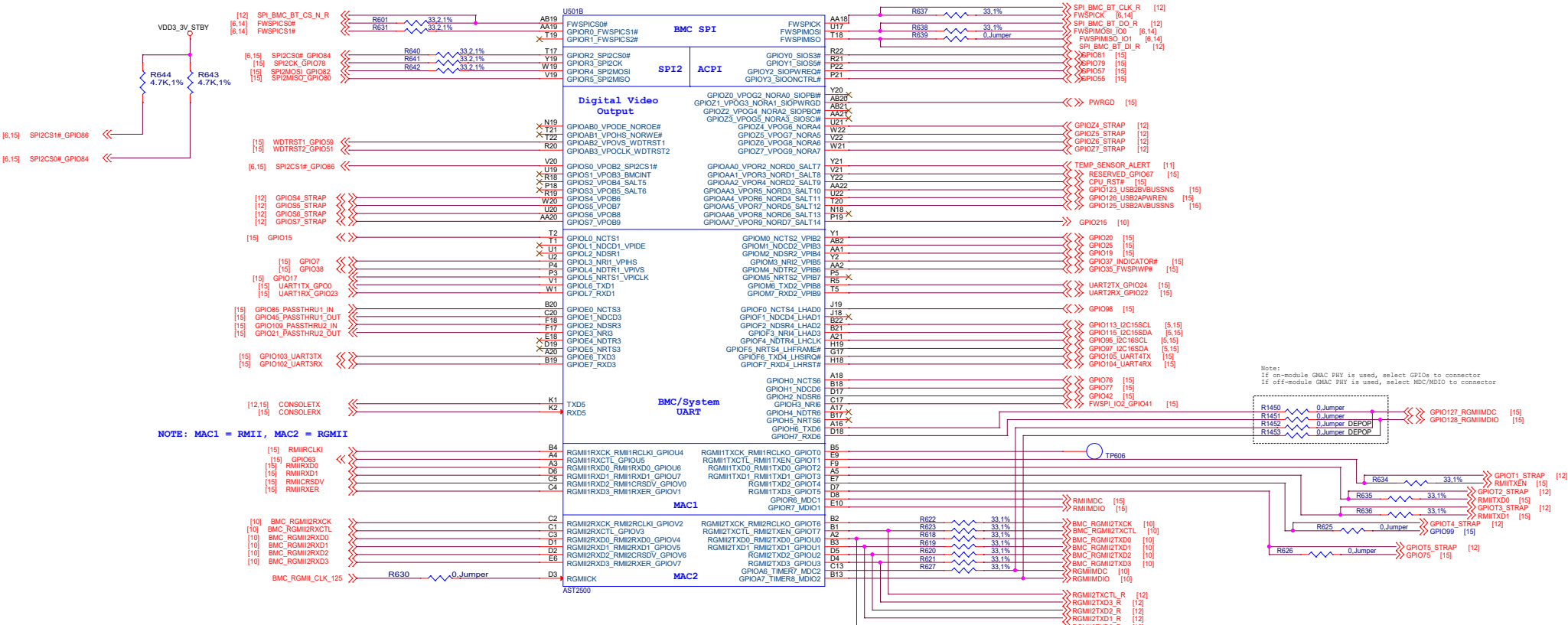
PS 1.15V



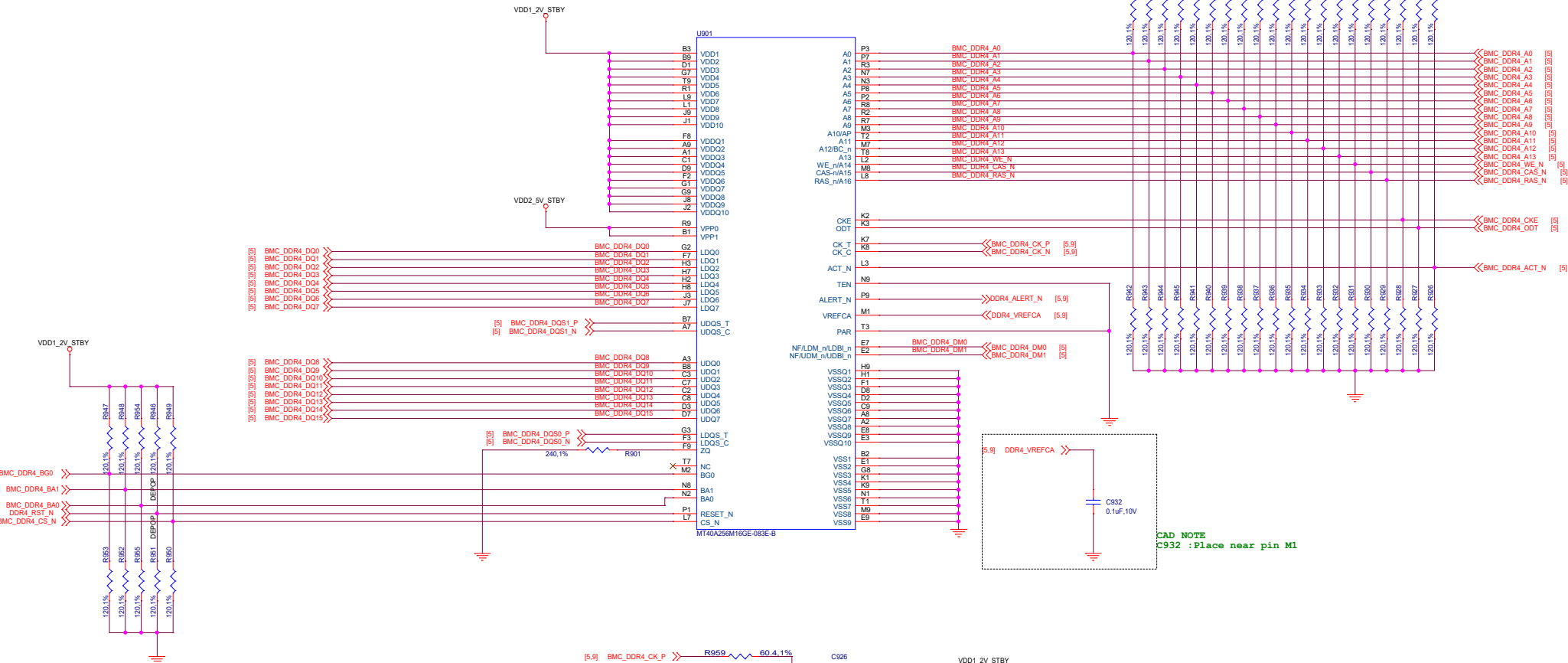
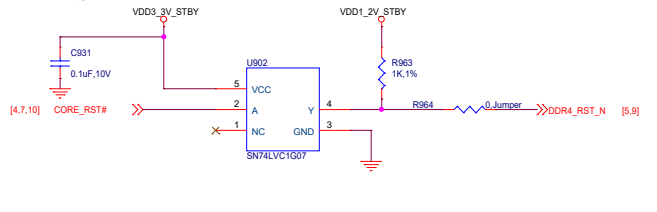
2.5V, 1.2V, 1.15V STBY POWER



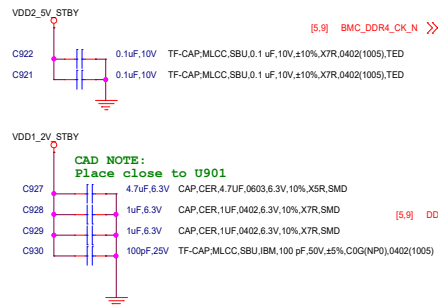
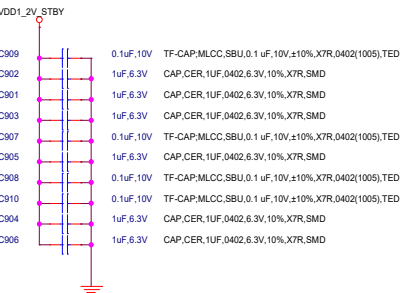
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DDR4 RESET

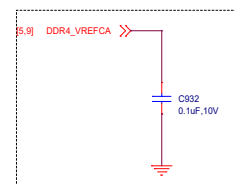


CAD NOTE:
Place these capacitors close to termination resistors



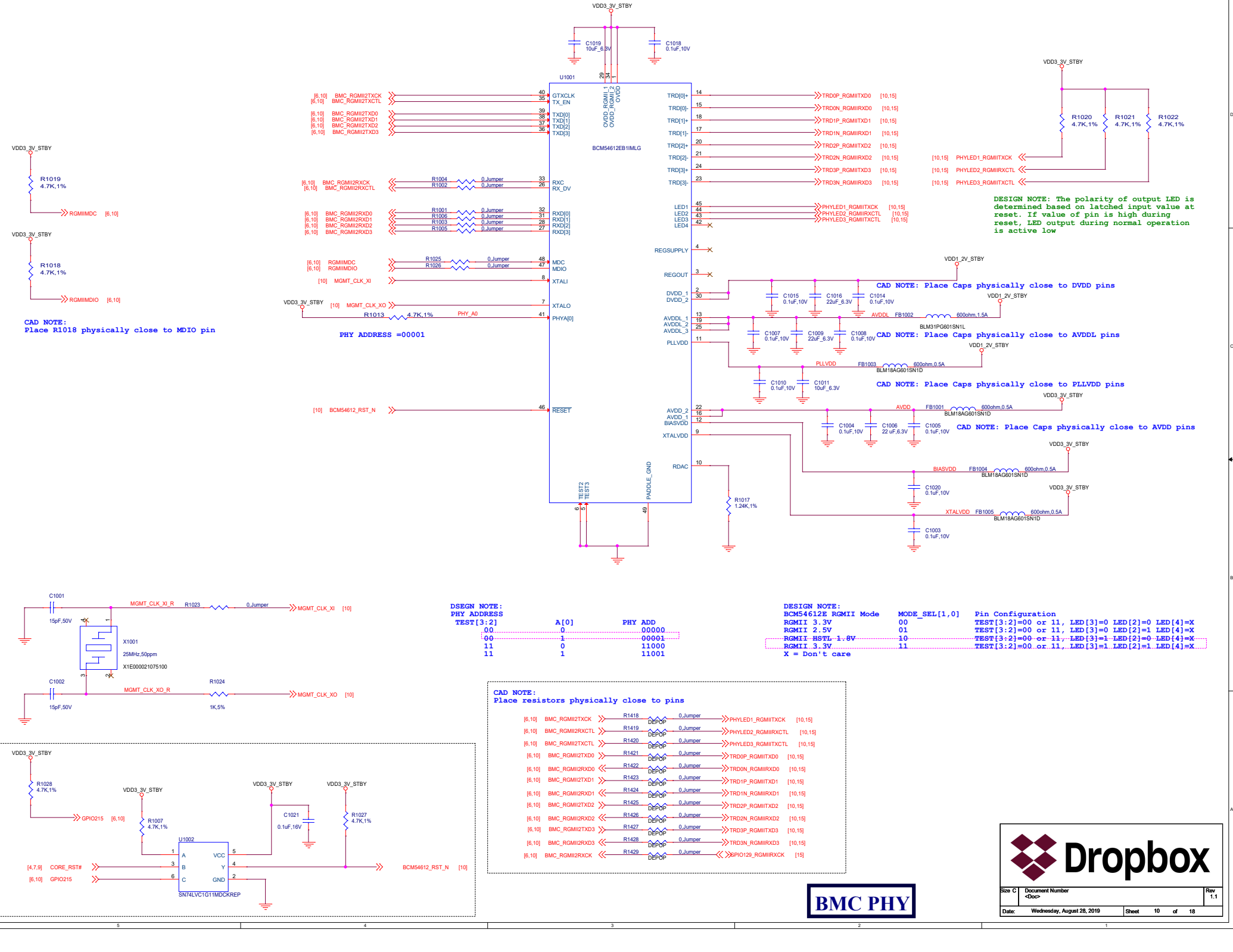
DESIGN NOTE
C924 :To prevent noise coupling from power

CAD NOTE: DDR4 VREFCA
Trace width must be greater than or equal to 15 mils



CAD NOTE
C932 :Place near pin M1

DDR4 RAM



CAD NOTE:
Place R1018 physically close to MDIO pin

CAD NOTE:
Place R1018 physically close to MDIO pin

DESIGN NOTE: The polarity of output LED is determined based on latched input value at reset. If value of pin is high during reset, LED output during normal operation is active low

CAD NOTE: Place Caps physically close to DVDD pins

CAD NOTE: Place Caps physically close to AVDDL pins

CAD NOTE: Place Caps physically close to PLLVDD pins

CAD NOTE: Place Caps physically close to AVDD pins

DSEGN NOTE:
PHY ADDRESS
TEST [3:2]

	A[0]	PHY ADD
00	0	00000
01	1	00001
11	0	11000
11	1	11001

DESIGN NOTE:

BCM54612E RGMII Mode	MODE_SEL[1,0]	Pin Configuration
RGMII 3.3V	00	TEST [3:2]=00 or 11, LED [3]=0 LED [2]=0 LED [4]=X
RGMII 2.5V	01	TEST [3:2]=00 or 11, LED [3]=0 LED [2]=1 LED [4]=X
RGMII_HSTL-1.8V	10	TEST [3:2]=00 or 11, LED [3]=1 LED [2]=0 LED [4]=X
RGMII 3.3V	11	TEST [3:2]=00 or 11, LED [3]=1 LED [2]=1 LED [4]=X

X = Don't care

CAD NOTE:
Place resistors physically close to pins

[6,10] BMC_RGMII2TXCK	R1418	0 Jumper	PHYLED1_RGMITXCK	[10,15]
[6,10] BMC_RGMII2RXCTL	R1419	0 Jumper	PHYLED2_RGMIRXCTL	[10,15]
[6,10] BMC_RGMII2TXCTL	R1420	0 Jumper	PHYLED3_RGMITXCTL	[10,15]
[6,10] BMC_RGMII2TXD0	R1421	0 Jumper	TRD0P_RGMITXD0	[10,15]
[6,10] BMC_RGMII2RXD0	R1422	0 Jumper	TRD0N_RGMIRXD0	[10,15]
[6,10] BMC_RGMII2TXD1	R1423	0 Jumper	TRD1P_RGMITXD1	[10,15]
[6,10] BMC_RGMII2RXD1	R1424	0 Jumper	TRD1N_RGMIRXD1	[10,15]
[6,10] BMC_RGMII2TXD2	R1425	0 Jumper	TRD2P_RGMITXD2	[10,15]
[6,10] BMC_RGMII2RXD2	R1426	0 Jumper	TRD2N_RGMIRXD2	[10,15]
[6,10] BMC_RGMII2TXD3	R1427	0 Jumper	TRD3P_RGMITXD3	[10,15]
[6,10] BMC_RGMII2RXD3	R1428	0 Jumper	TRD3N_RGMIRXD3	[10,15]
[6,10] BMC_RGMII2RXCK	R1429	0 Jumper	GPIO129_RGMIRXCK	[15]

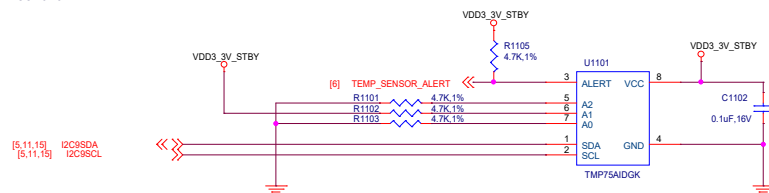
BMC PHY



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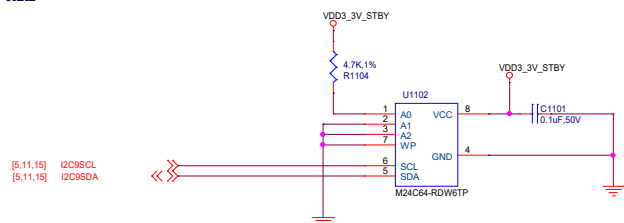
TEMP SENSOR

I2C ADDRESS=0X94



EEPROM

I2C ADDRESS=0XA2



BOM Note:

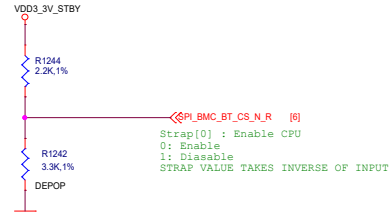
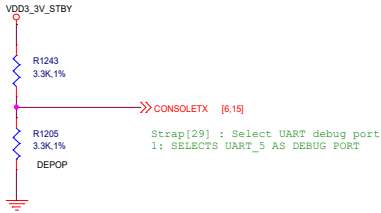
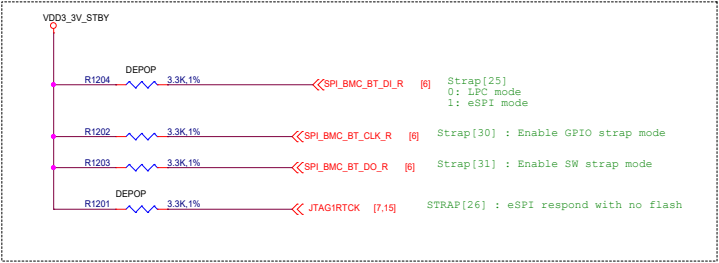
change U1102 from AT24C64D-SSHM-T (H=1.75mm)
to ST/ M24C64-RDW6TP (H=1mm)

TEMP SENSOR, EEPROM

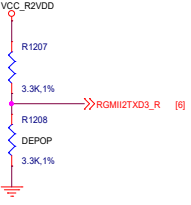


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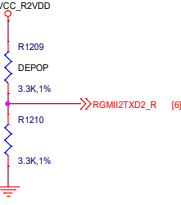
BMC STRAPPING - DESIGN NOTES



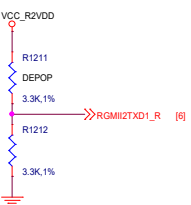
Strap[24]: Select DDR4 SDRAM, 1: DDR4 SDRAM



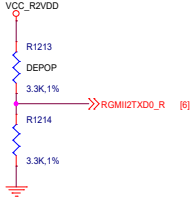
Strap[23]: Select CLKIN = 25 MHz mode, 0: CLKIN = 24 MHz and USBCKI not used



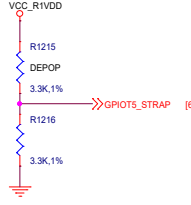
Strap[22]: Enable GPIOE pass-through mode, 0: Disable



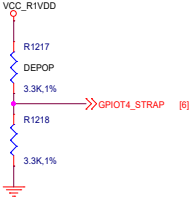
Strap[21]: Enable GPIOD pass-through mode, 0: Disable



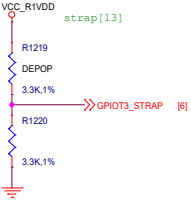
Strap[19]: Enable ACPI function pins, 0: Disable



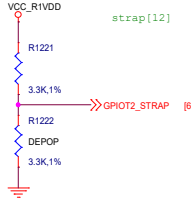
Strap[16]: SuperIO configuration address selection, 0: 0x2E, 1: 0x4E



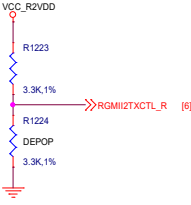
Strap[13:12]: SPI1 mode selection, 00: GPIO mode, 01: SPI master, 10: Reserved, 11: SPI pass-through



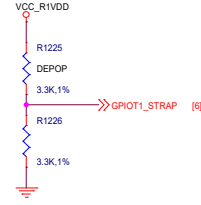
strap[12]



Strap[7]: Select MAC #2 RGMII mode, 0: RGMII/ NCSI, 1: RGMII



Strap[6]: Select MAC #1 RGMII mode, 0: RGMII/ NCSI, 1: RGMII



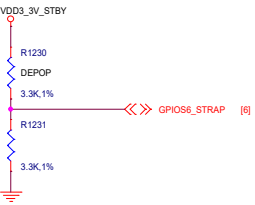
Strap[4]: RESERVED, 0: DEFAULT



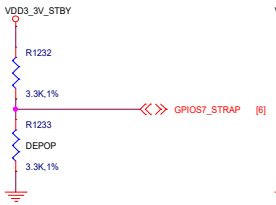
Strap[3]: VGA MEMORY SIZE SELECTION, 0: 16 MB, 1: 64 MB



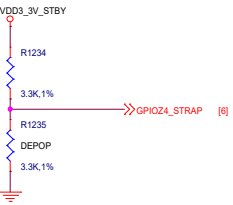
Strap[5]: VGA BIOS ROM, 0: DISABLE, 1: ENABLE



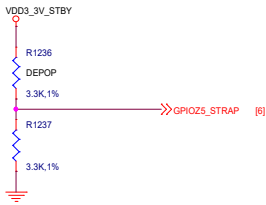
Strap[15]: VGA CLASS CODE SELECTION, 0: NON - VGA, 1: VGA



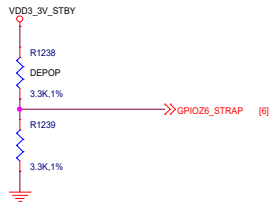
Strap[17]: BMC SECOND BOOT WATCHDOG TIMER, 0: DISABLE, 1: ENABLE



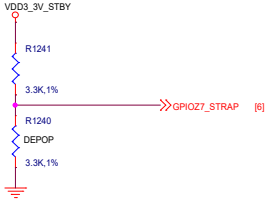
STRAP[18]: USBCKI INPUT FREQUENCY, 0: 24 MHz, 1: 48 MHz



Strap[20]: DISABLE LPC TO DECODE SUPER IO ADDRESS, 0: NO



Strap [27]: ENABLE FAST RESET MODE, 1: YES



BMC STRAPPING

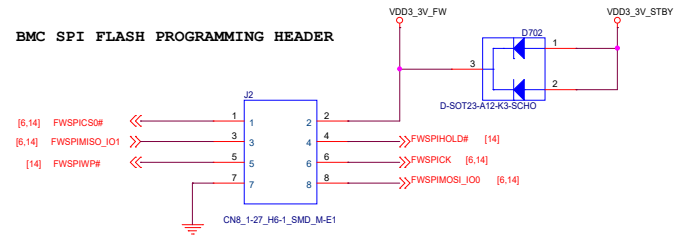
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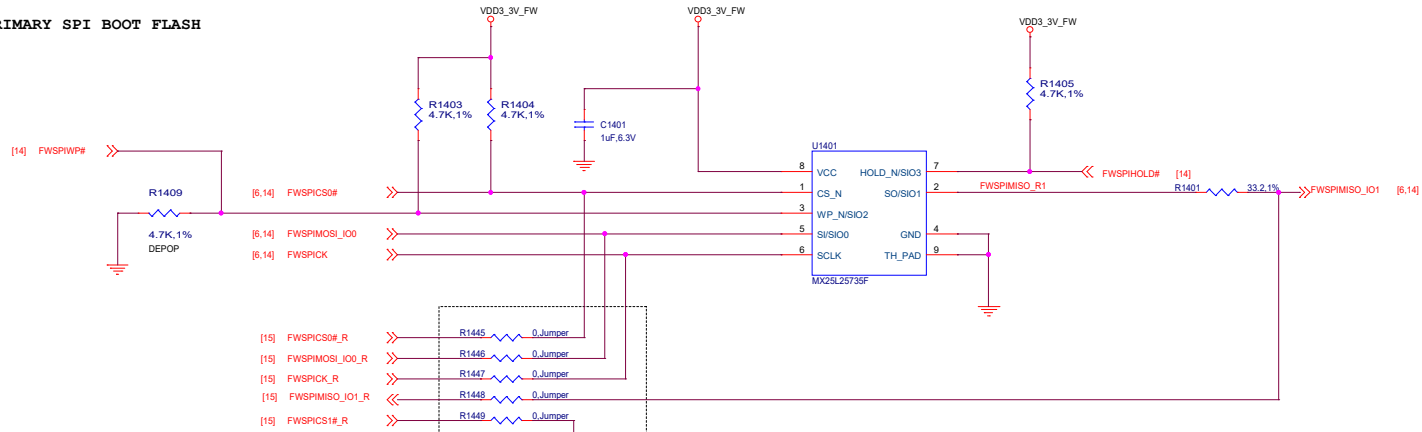
PIN NUMBER	PIN NAME	NET NAME	STRAP BIT NO.	INTERNAL PUI/PD	VALUE	DESCRIPTION
AB19	FWSPICS0#	SPL_BMC_BT_CS_N	STRAP[0]	PU	0	1: DISABLE CPU [STRAP VALUE TAKES INVERSE OF INPUT] 0: Enable CPU
AA18	FWSPICK	SPL_BMC_BT_CLK_R	STRAP[30]	PD	1	1: Enable GPIO strap mode 0: Disable
U17	FWSPIMOSI	SPL_BMC_BT_DQ_R	STRAP[31]	PD	1	1: Enable SW strap mode 0: Disable
T18	FWSPIMISO	SPL_BMC_BT_DI	STRAP[25]	PD	0	1: Enable espi 0: LPC mode
C9	RTCK	BMC_JTAG_RTCK	STRAP[26]	PD	1	1: Enable eSPI flash mode 0: eSPI respond with no flash attached
K1	TXD5	UART_TXD5	STRAP[29]	PU	1	1: Select UART5 as BMC console port 0: Select UART1 as BMC console port
E9	RMII1TXEN_R	GPIO1_STRAP	STRAP[6]	PD	0	1: Select MAC #1 RGMII mode 0: Select MAC #1 RGMII/ NCSI mode
B1	RGMII2TXCTL_R	RGMII2TXCTL_R	STRAP[7]	PD	1	1: Select MAC #2 RGMII mode 0: Select MAC #2 RGMII/ NCSI mode
A5	RMII1TXD1_R	GPIO3_STRAP	STRAP[13]	PD	0	Strap[13:12]: SPI1 mode selection
F9	RMII1TXD0_R	GPIO2_STRAP	STRAP[12]	PD	1	00: GPIO mode 01: SPI master 10: Reserved 11: SPI pass-through
E7	GPIO4	GPIO4_STRAP	STRAP[16]	PD	0	SuperIO configuration address selection 0: 0x2E 1: 0x4E
D7	GPIO5	GPIO5_STRAP	STRAP[19]	PD	0	1: Enable ACPI function pins 0: Disable
A2	RGMII2TXD0_R	RGMII2TXD0_R	STRAP[21]	PD	0	1: Enable GPIOD pass-through mode 0: Disable
B3	RGMII2TXD1_R	RGMII2TXD1_R	STRAP[22]	PD	0	1: Enable GPIOE pass-through mode 0: Disable
D5	RGMII2TXD2_R	RGMII2TXD2_R	STRAP[23]	PD		1: Select CLKIN = 25 MHz and USBCKI = 24/48 MHZ 0: CLKIN= 24 MHZ and USBCKI not used
D4	RGMII2TXD3_R	RGMII2TXD3_R	STRAP[24]	PD	1	1: Select DDR4 SDRAM 0: Select DDR3 SDRAM
R19	GPIO54	GPIO54_STRAP	STRAP[3]	PD	0	VGA memory size selection 1: 64MB 0: 16MB
W20	GPIO55	GPIO55_STRAP	STRAP[4]	PD	0	Reserved
U20	GPIO56	GPIO56_STRAP	STRAP[5]	PD	0	1: Enable VGA BIOS ROM 0: Disable
AA20	GPIO57	GPIO57_STRAP	STRAP[15]	PD	1	1: VGA Class code selection 0: Non - VGA Class code selection
U21	GPIO24	GPIO24_STRAP	STRAP[17]	PD	1	1: Enable BMC second boot watchdog timer 0: Disable
W22	GPIO25	GPIO25_STRAP	STRAP[18]	PD	0	USBCKI INPUT FREQUENCY 1: 48 MHZ 0: 24 MHZ
V22	GPIO26	GPIO26_STRAP	STRAP[20]	PD	0	1: Disable LPC to decode super IO address 0: Enable
W21	GPIO27	GPIO27_STRAP	STRAP[27]	PD	1	1: Enable fast reset mode 0: Long reset mode, normal operation



BMC SPI FLASH PROGRAMMING HEADER

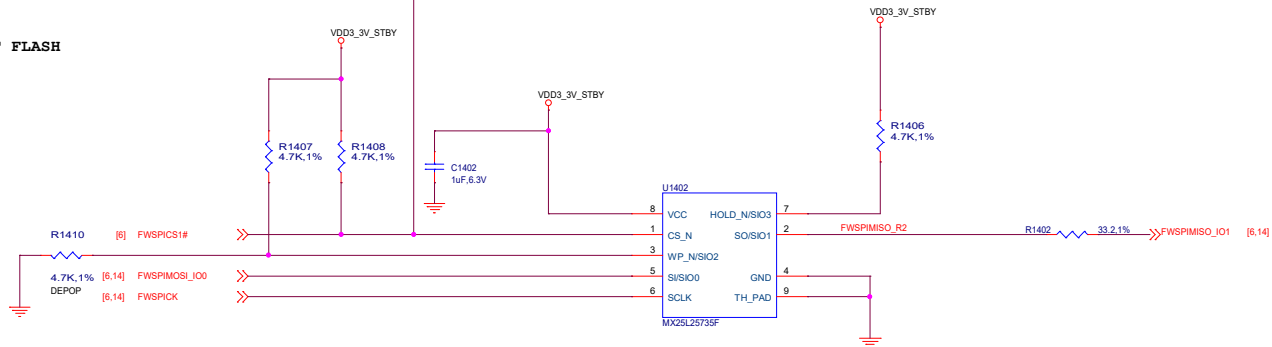


PRIMARY SPI BOOT FLASH



Note: Depop these resistors for security concerns and isolate the FWSP1 from the Host system

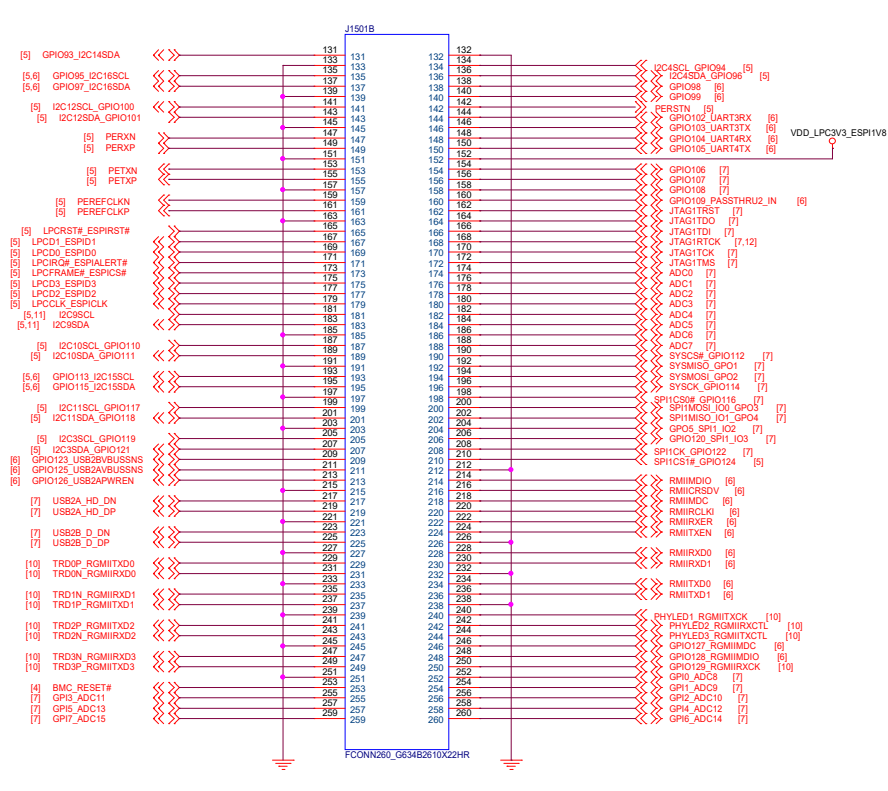
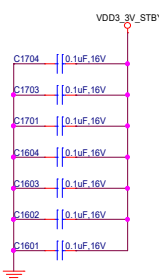
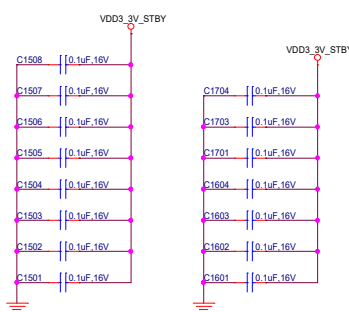
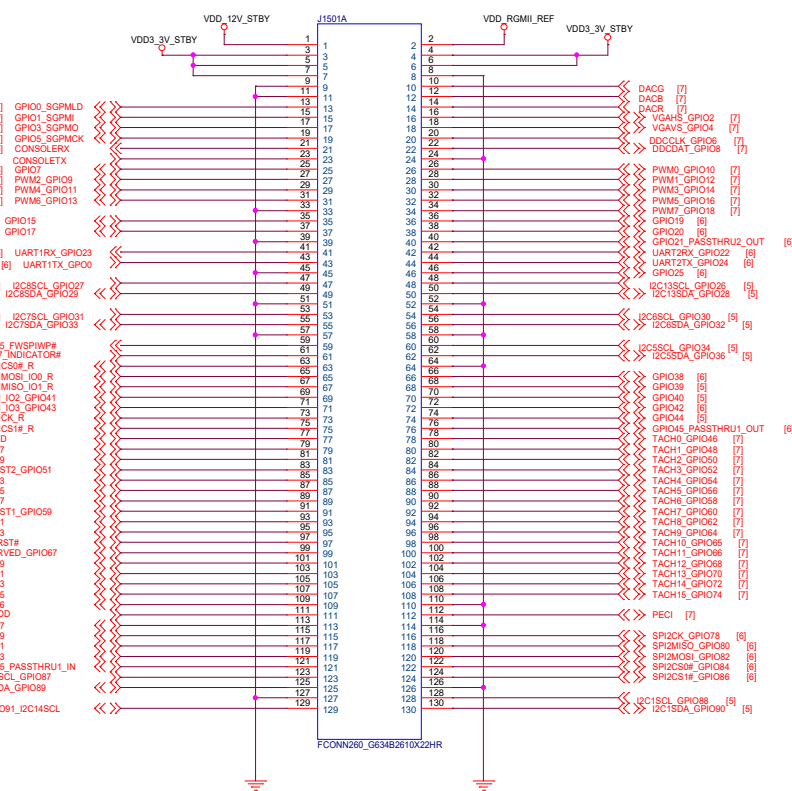
SECONDARY SPI BOOT FLASH



SPI BOOT FLASH



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CONNECTOR - 1



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REVISION HISTORY

Revision History - DVT

@2019/1/16

- 1 FWSPI doesn't provide GPIO functionality. Removed resistors (R1413/R1414/R1415/R1416/R1417)
- 2 Route FWRGD (pin 77 on connector) to ball AB20 on AST2500
- 3 Place 150 Ohm (R1440/R1441/R1442) termination near AST2500 SoC for DACG, DACR, and DACB signals
- 4 Change pin names on 260p golden fingers based on OCP_RunBMC_Pinout_Specification_01.

@2019/2/11

- 5 X1001, replace X1E000021064800 with X1E000021075100; C1001,C1002, replace 22pf with 15pf; R1024 replace 0ohm with 1kohm, for better xtal performance.

@2019/4/25

change the net name from KLUDGE_GPIO63 to CPU_RST#

@2019/5/9

Place a 33.2 series resister on net SPI1CS0#_GPIO116 and SPI1MISO_IO1_GPO4

@2019/5/23

- 1.Rename "KLUDGE_GPIO65" net to "RESERVED_GPIO65"
- 2.Add wired OR resistors option to support GPIO127/128 for net RGMIMDC/RGMIMDIO in case MDC/MDIO communicate wtih on-chip PHY: R1450:R1453
- 3.Add FWSPI isolation resistors from connector for sercurity concern: R1445:R1449
- 4.Depop I2C pull-up resistors, R501:R520, R524, R525, R528, R529, R1430:R1435

@2019/5/27

- 1.Change GPIO127/128 support from GPIOH4/5 to GPIOH6/7

@2019/6/10

1. Adding secondary functions to support pass-through
Connect J1501A.35 to GPIOE0
Connect J1501A.36 to GPIOE1
Connect J1501A.37 to GPIOE2
Connect J1501A.38 to GPIOE3
2. Move U1101 and U1102 to I2C9 from I2C13,
Pop R517/R518 for I2C9
Depop R526/R527 for I2C13

@2019/08/08

1. assign GPIO83/43/107/21 to be passthru function to GPIO Group E in BMC
Connect J1501A.121 to GPIOE0
Connect J1501A.76 to GPIOE1
Connect J1501A.160 to GPIOE2
Connect J1501A.40 to GPIOE3
2. connect GPIO15/19/17/20 back to where they were GPIOI0/M2/L5/M0
Connect J1501A.35 to GPIOI0
Connect J1501A.36 to GPIOM2
Connect J1501A.37 to GPIOI5
Connect J1501A.38 to GPIOM0

@2019/08/26

GPIO pin number change to match pinout v1.4

@2019/09/10

Modify block diagram to meet the schematic design on page 2 and 3

REVISION HISTORY

