

01 INDEX

02 BLANK

03 EDGE CONNECTOR

04 CONNECTOR - 1

05 CONNECTOR - 2

06 CONNECTOR - 3

07 JTAG,PWM,LPC,GPIO,PECI,LPC

08 USB

09 UART CONSOLE

10 PHY BCM5221

11 ETHERNET CONNECTOR

12 VGA DB15 CONNECTOR

13 I2C, WATCHDOG RST HEADER

14 IO EXPS, POWER METER

15 TSENSOR, EEPROM, I2C EXP

16 I2C, IO EXP CONNECTOR

17 SPI

18 RESET CIRCUIT, ADC HEADERS

19 TACH, PWM

20 MUX/ DEMUX SWITCHES, FT232, USB CONN

21 MUX/ DEMUX SWITCHES, FT232, USB CONN

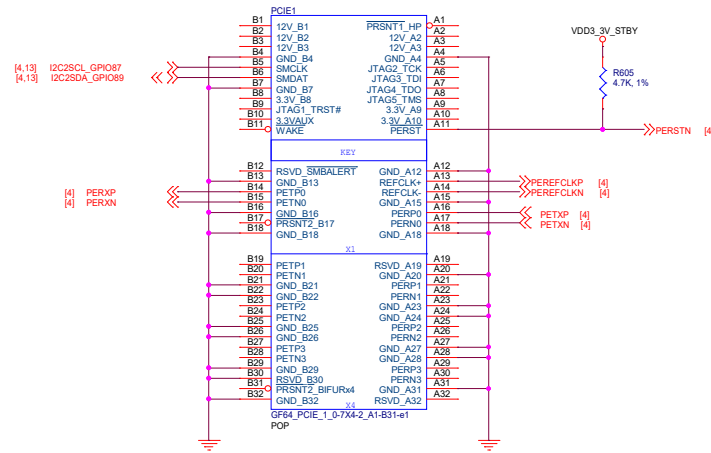
22 POWER 5V

23 POWER 3.3V

24 VDD_5V POWER SWITCH

25 REVISION HISTORY

THIS PAGE WAS INTENTIONALLY LEFT BLANK

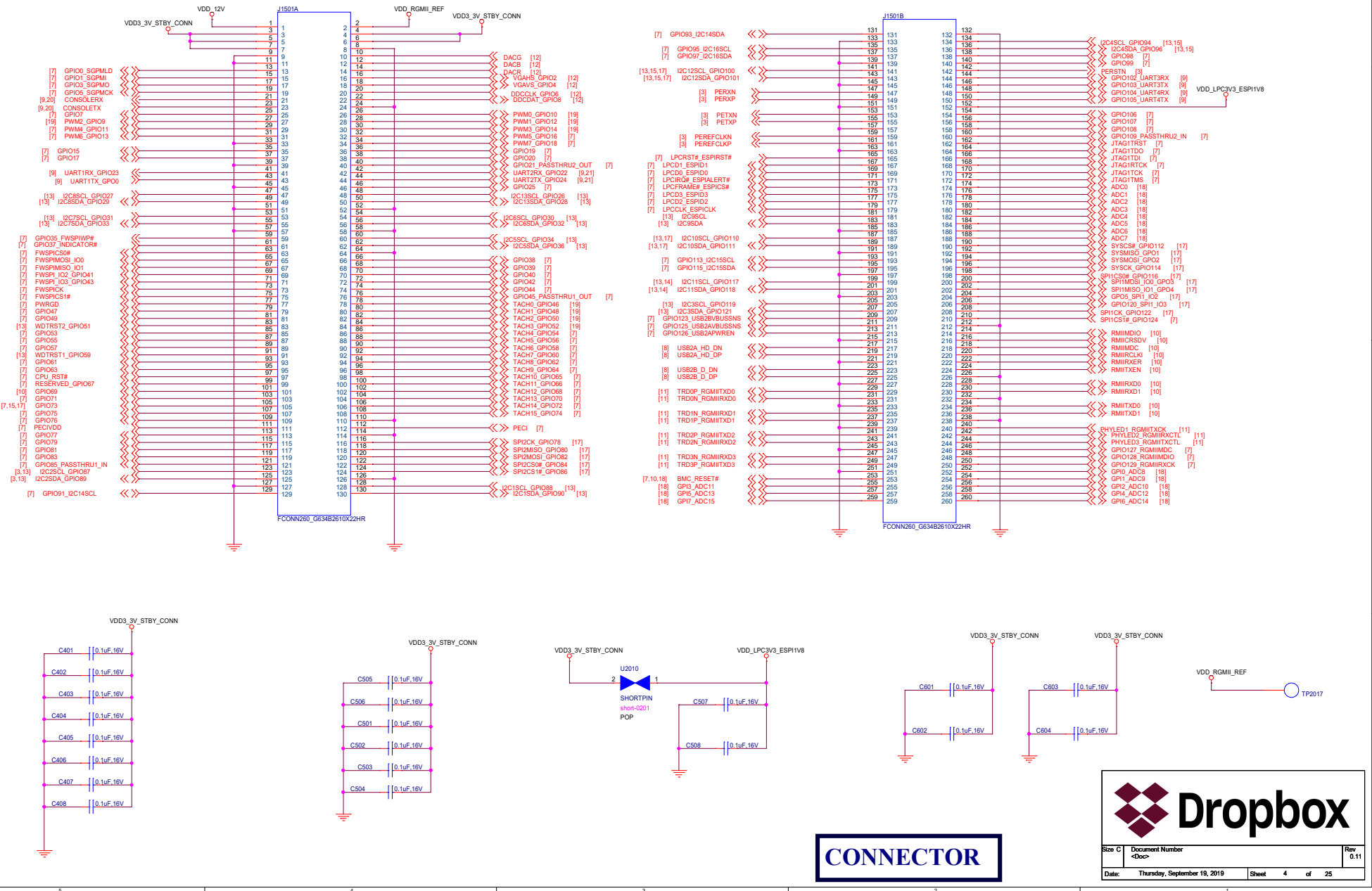


PCIe GF



Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 3 of 25

BOM Note: Changed J1501 TO G634B2610422HR



THIS PAGE WAS INTENTIONALLY LEFT BLANK


CONNECTOR

**Dropbox**

Size C	Document Number	Rev
	<Doc>	0.11
Date:	Thursday, September 10, 2019	Sheet 5 of 25

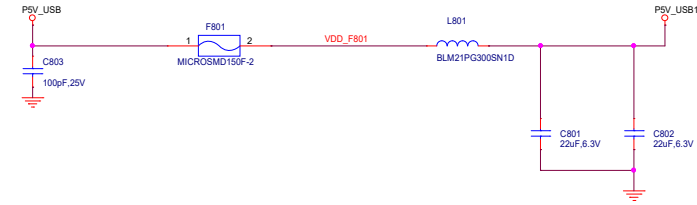
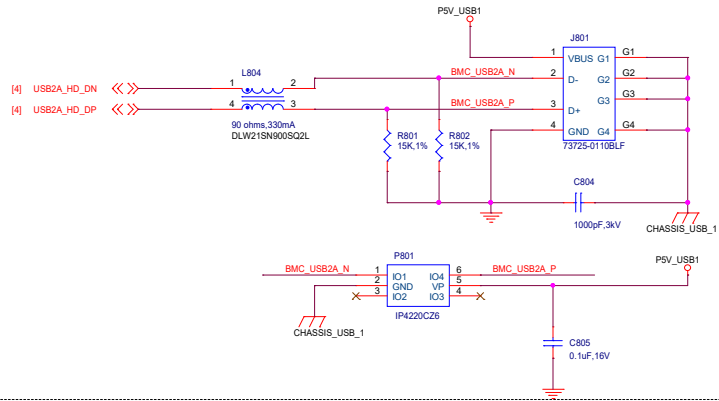
THIS PAGE WAS INTENTIONALLY LEFT BLANK

CONNECTOR

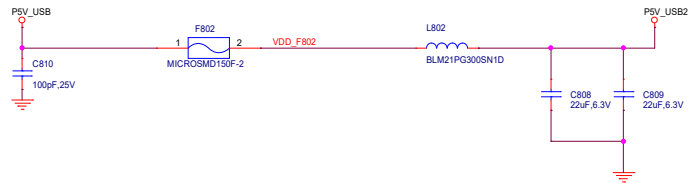
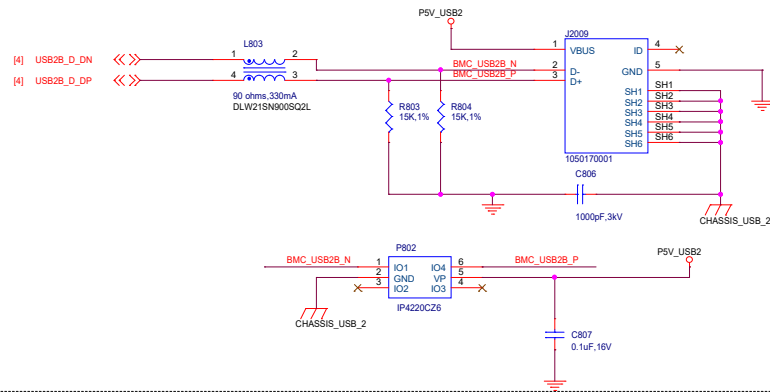
**Dropbox**

Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 6 of 25

TYPE A USB PORT-1



USB PORT-2/ MICRO USB

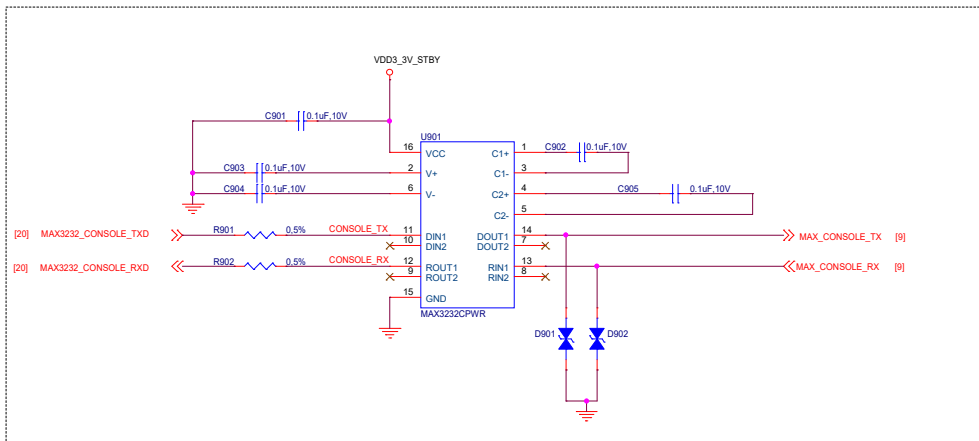


USB CONNECTOR

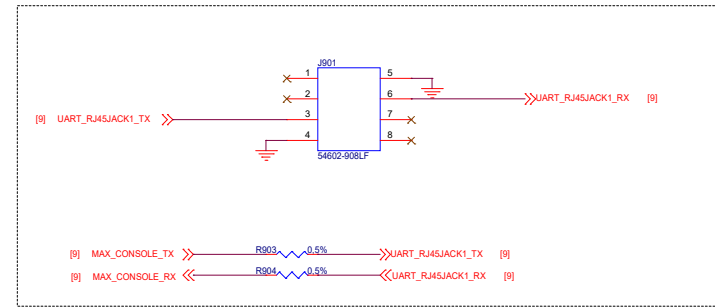


Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 10, 2019	Sheet 8 of 25

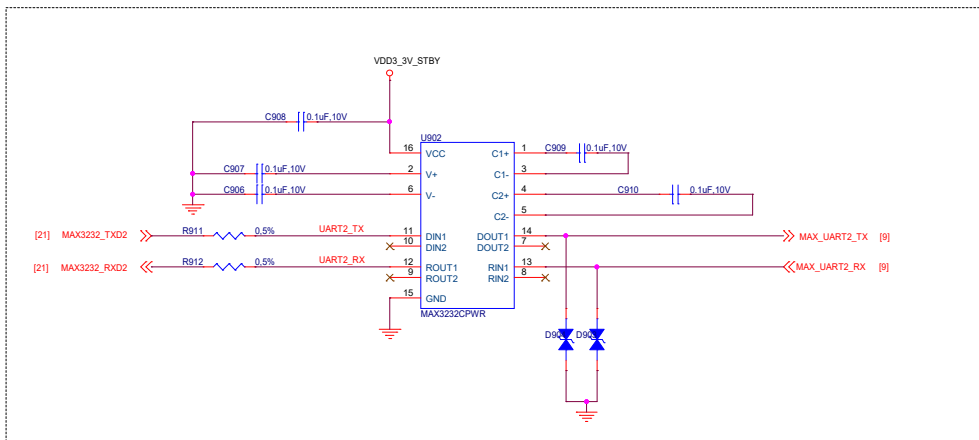
MAX 3232 -1



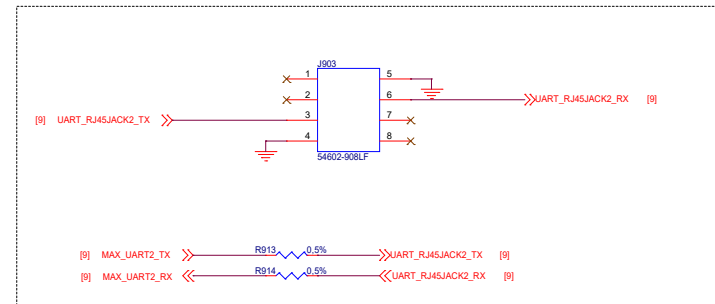
UART CONSOLE -1



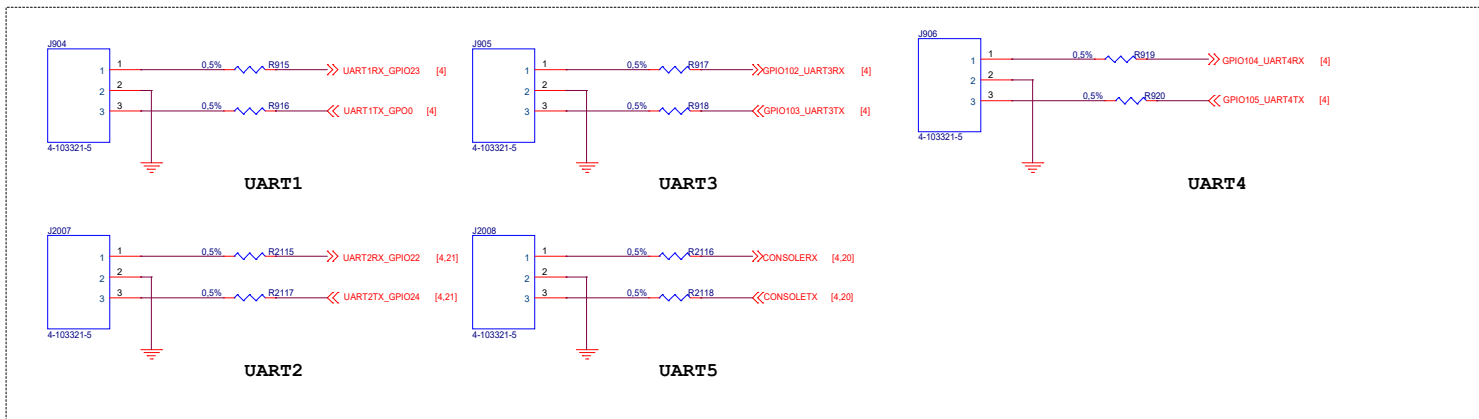
MAX 3232 -2



UART CONSOLE -2



UART HEADER

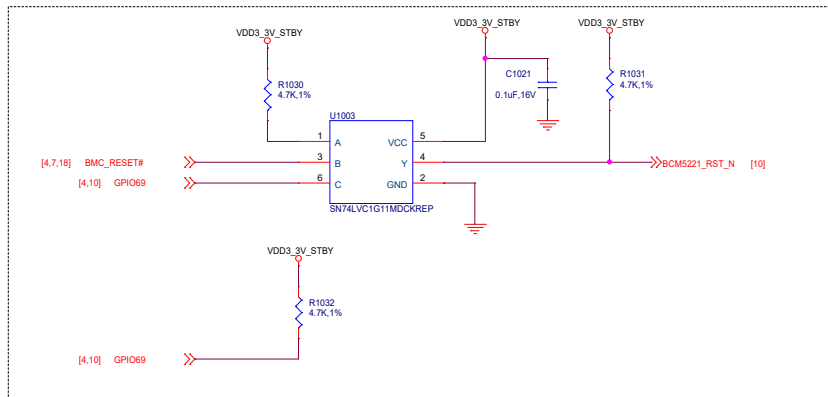


UART CONSOLE



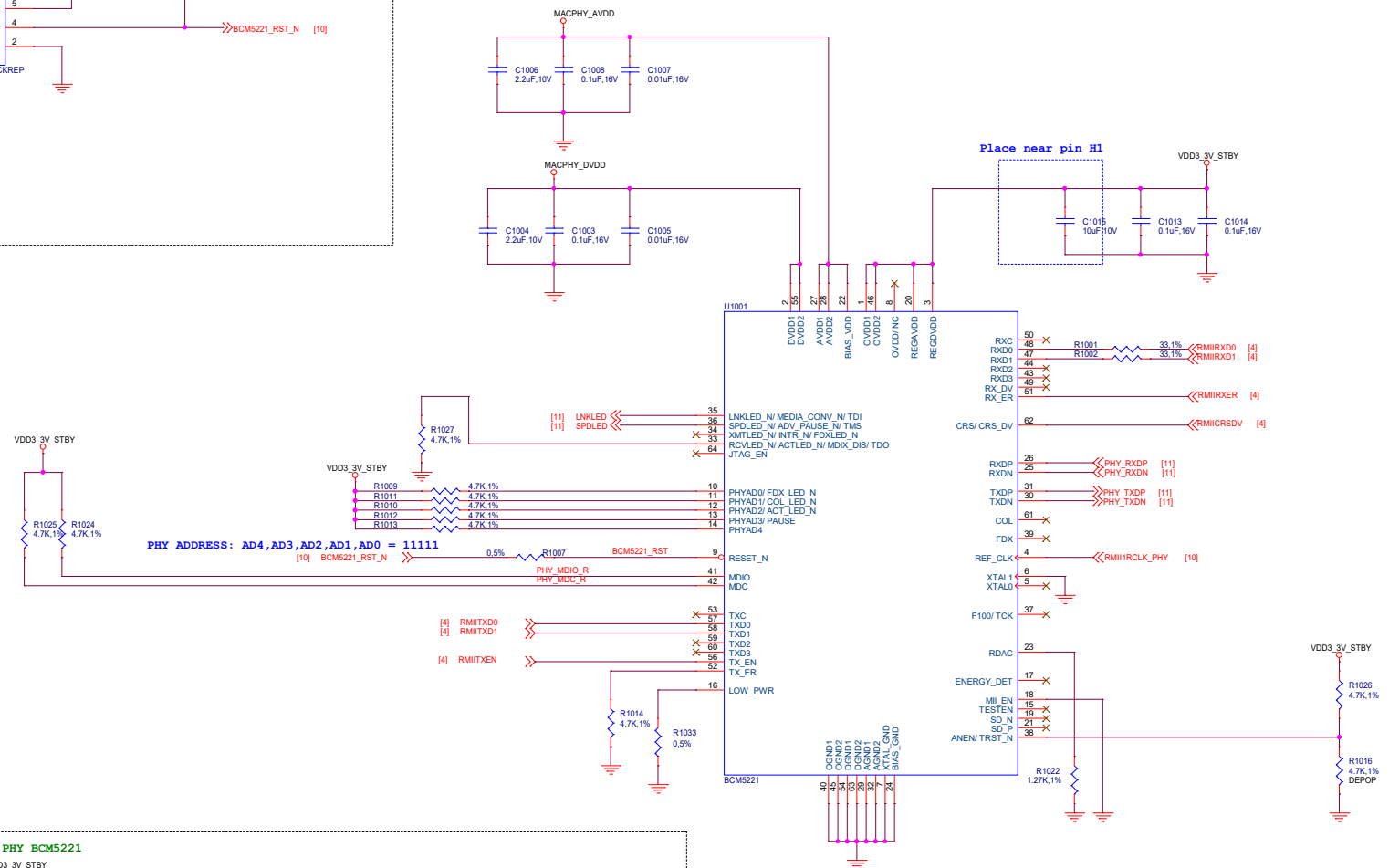
Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 9 of 25

RESET CIRCUIT



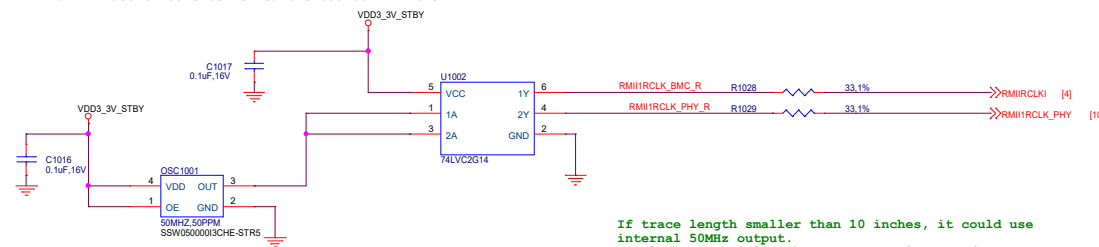
BOM Note:

Changed U1001 from BCM5221KPB to BCM5221A4KPTGT, changed the package from FBGA to TQFP



CLOCK CIRCUIT

NOTE: Place thiss clock circuit close to PHY BCM5221



BOM NOTE:

Changed OSC1001 from CWX823-050.0M
to HELE SSW050000I3CHE-STR5 for material
shortage issue

If trace length smaller than 10 inches, it could use internal 50MHz output.
For longer trace length, use external OSC and balance the clock trace length to both targets within 4 inches difference

[4] RMIIMDC >> TP1001

[4] RMIIMDIO >> TP1002

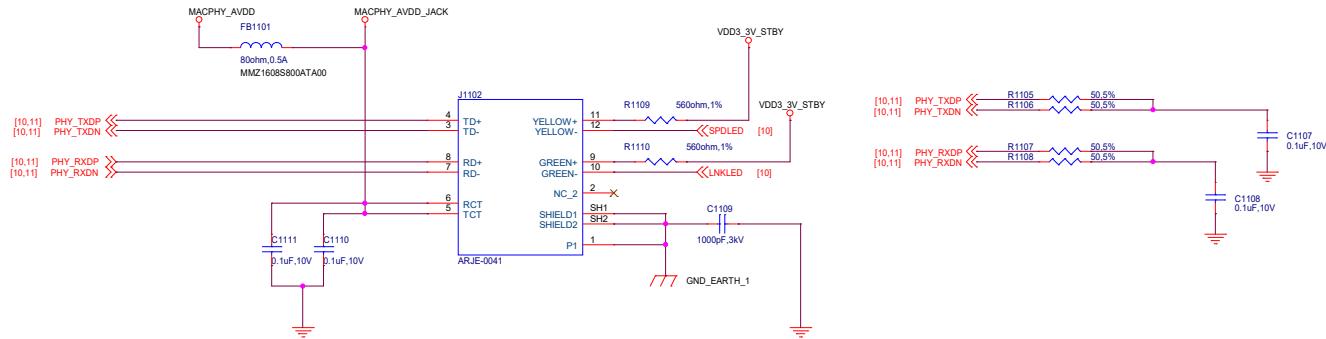
PHY



Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 10 of 25

RMII RJ45 ETHERNET JACK

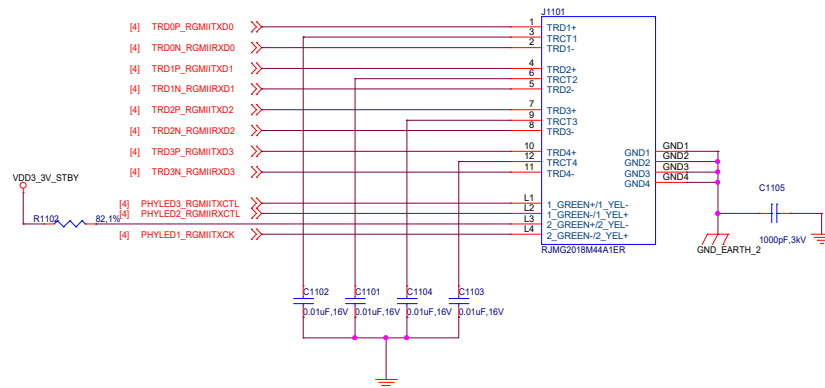
From A PHY ON HSBUV



CAD NOTE: Add layout silkscreen RMII / MAC2

RGMI RJ45 ETHERNET JACK

From RunBMC Module



CAD NOTE: Add layout silkscreen RGMII / MAC1

BOM Note: Changed J1101 from L829-1J1T-43 to RJMG2018M44A1ER

ETHERNET CONNECTOR

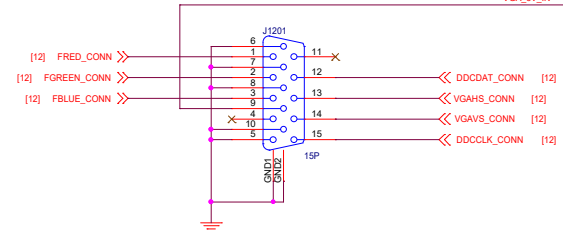
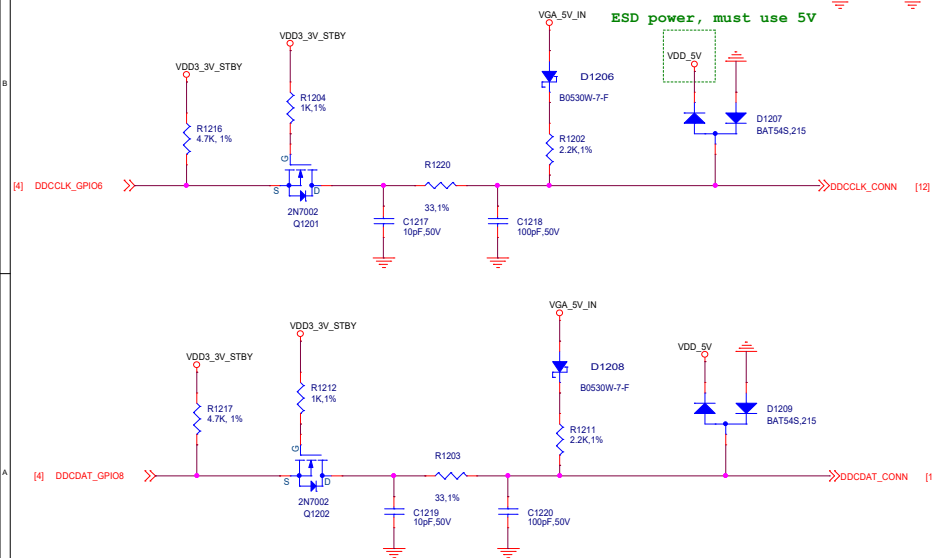
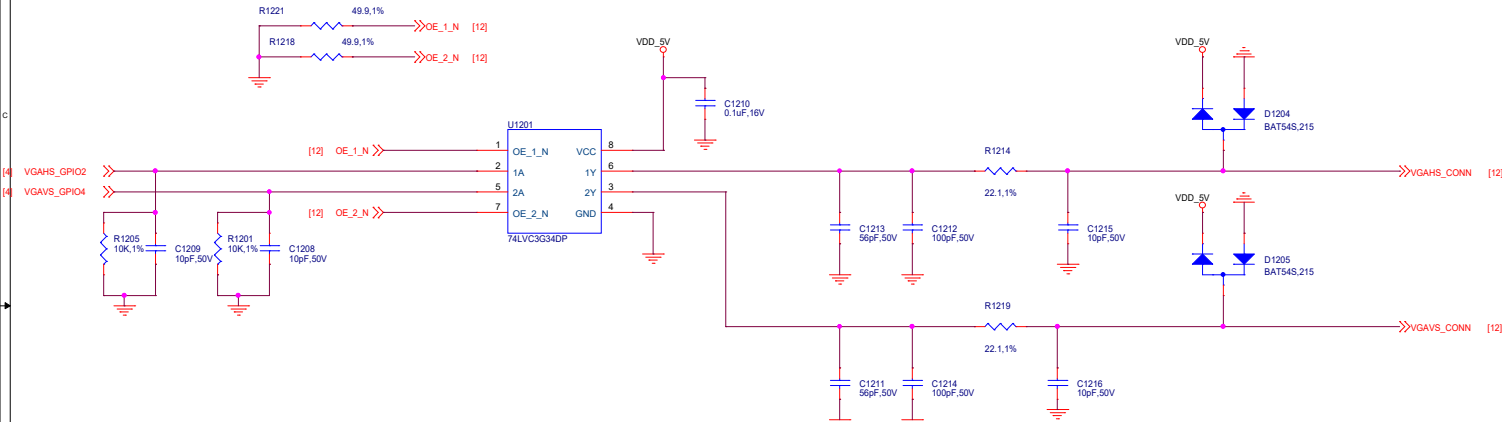
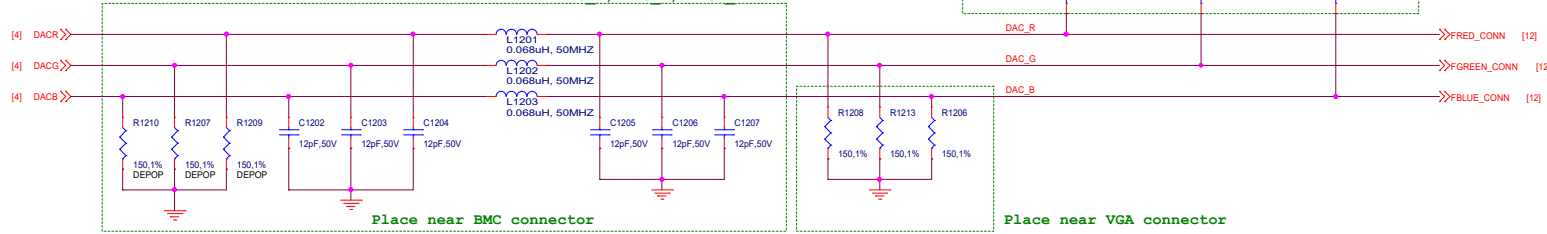


Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 10, 2019	Sheet 11 of 25

Design Note:
150 ohm termination for R/G/B are reserved on RunBMC Module and HSBUV
Pop 150 ohm on RunBMC Module and de-pop 150 ohms on HSBUV (Default)

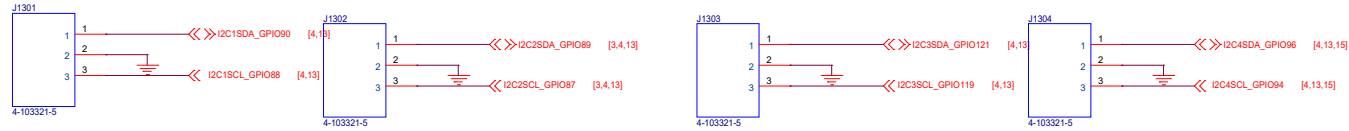
Design Note:
Trace impedance : 50 ohm
DACR, DACG, DACB
DAC_R, DAC_R, DACB_R

ESD, Place near VGA connector

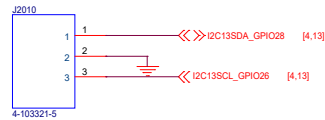
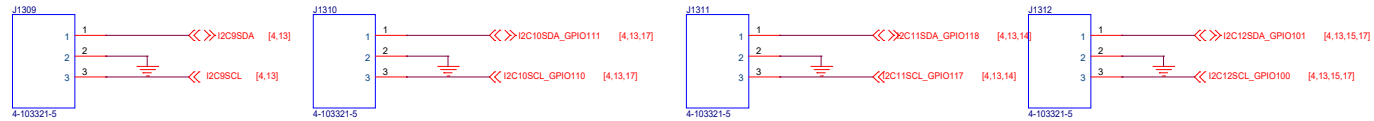
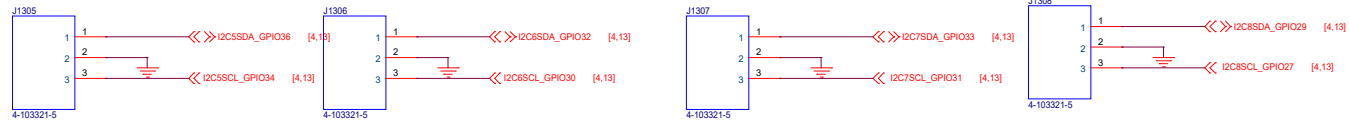


VGA DB15

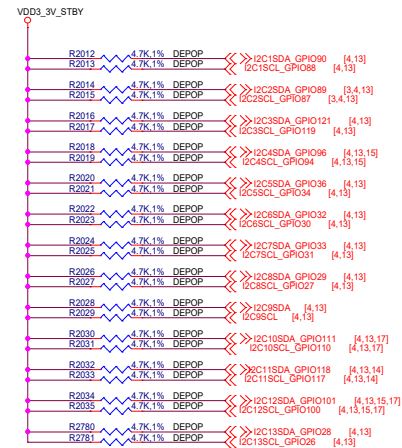
I2C



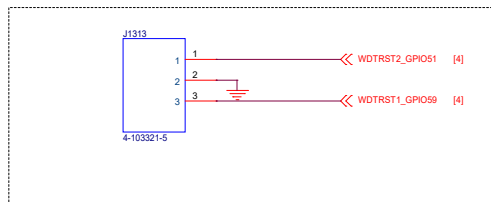
NOTE: Add sikscreen designators for J1301,1302,1303 (I2C1, I2C2, I2C3)



PULLUP FOR I2C SIGNALS



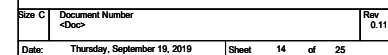
WDRST



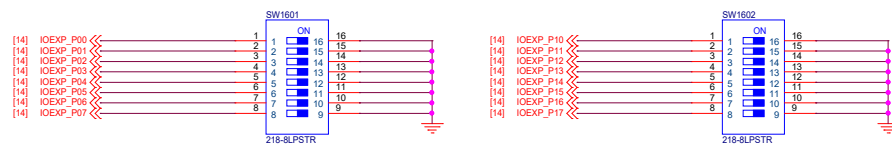
I2C HEADER, WDRST



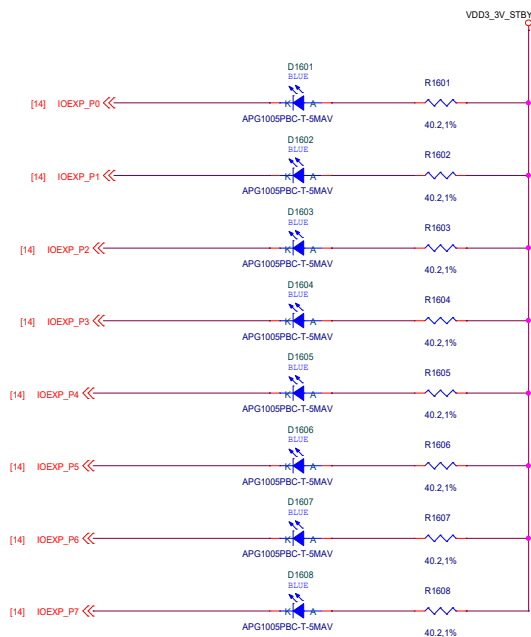
Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 13 of 25

[illegible]

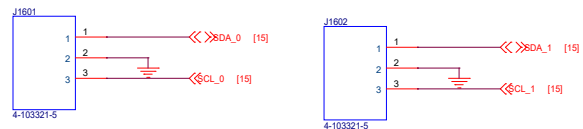
16 BIT I/O EXPANDER



8 BIT I/O EXPANDER



I2C EXPANDER

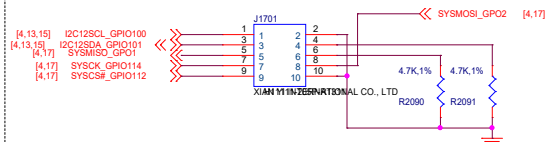


I2C, IO EXP

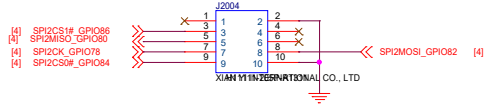


Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 10, 2019	Sheet 16 of 25

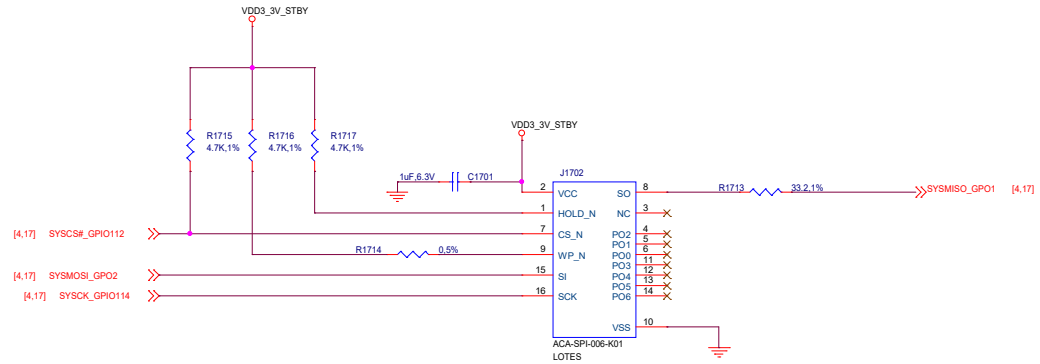
SYS SPI HEADER



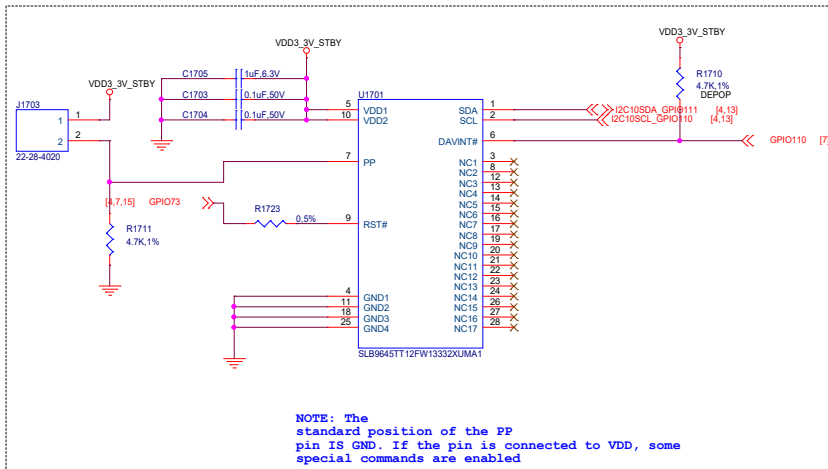
SPI2 HEADER



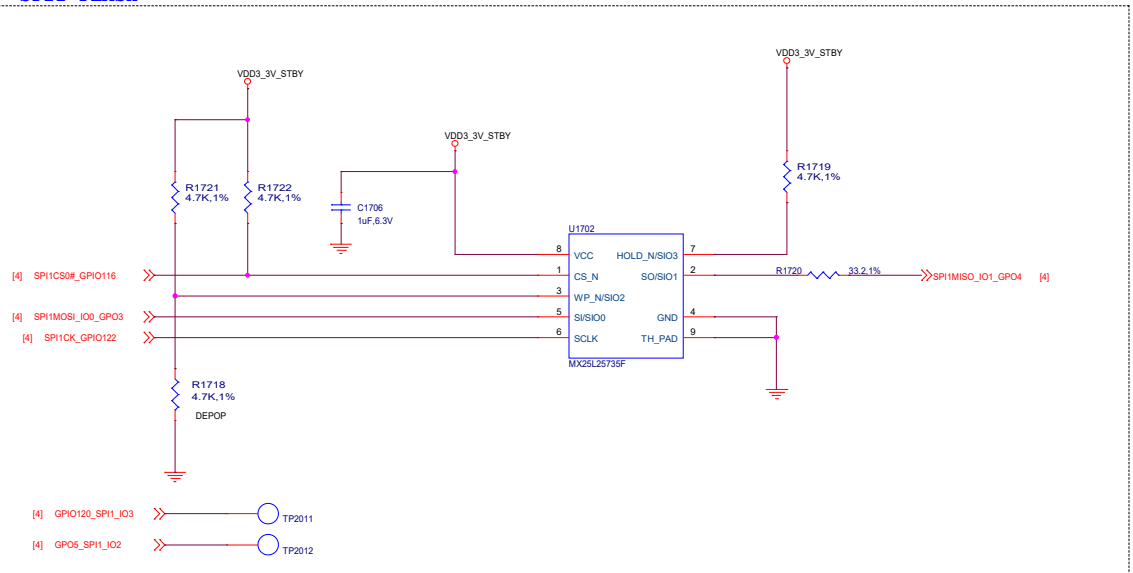
SPI_SYS FLASH SOCKET



TPM BASED I2C

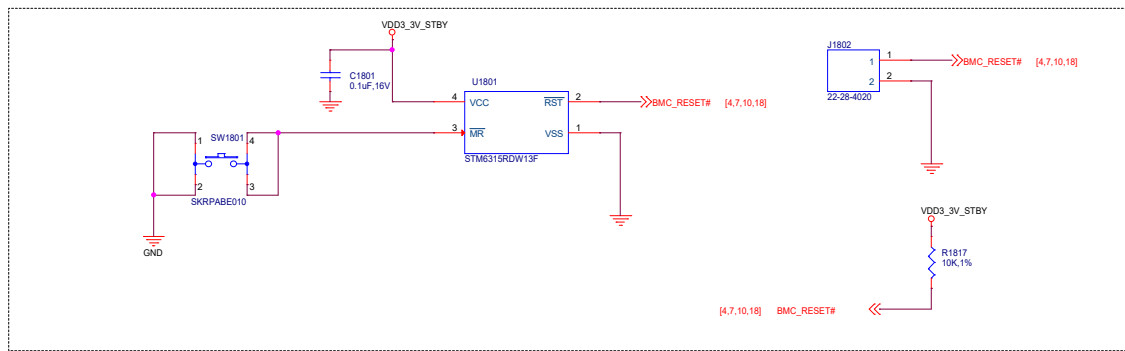


SPI1 FLASH

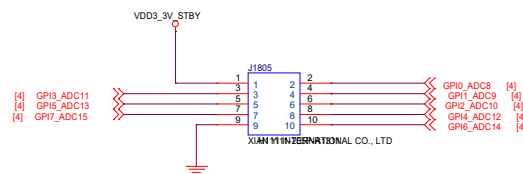
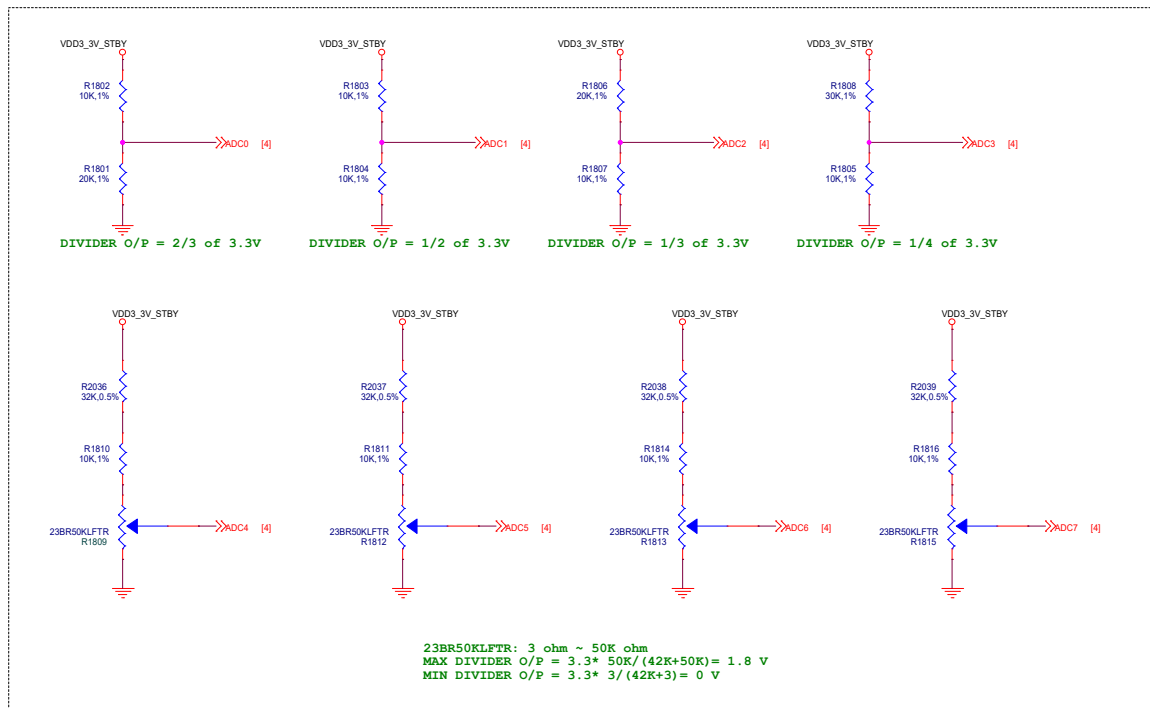


SPI EEPROM

BMC RESET



ADC



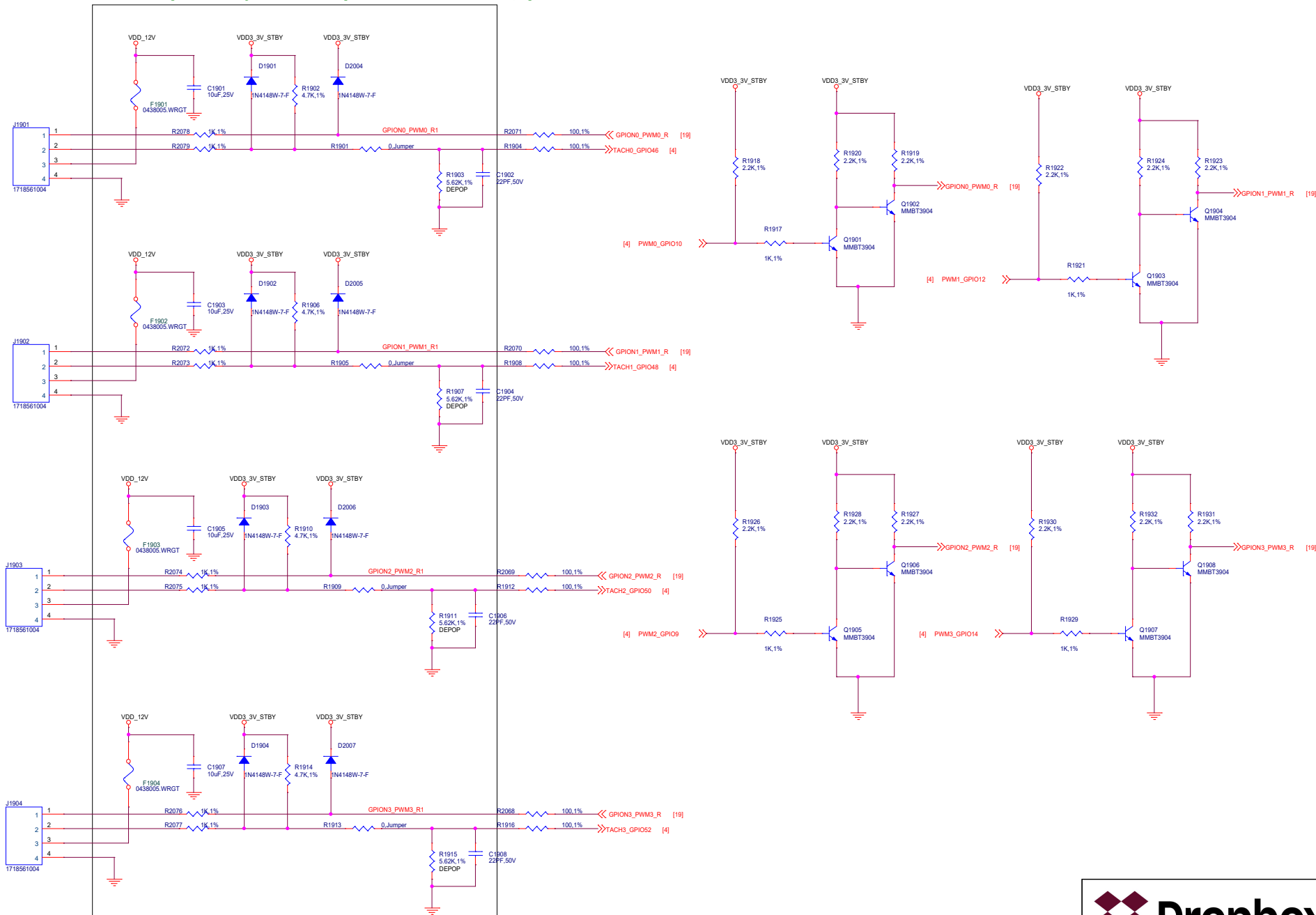
BMC RESET, ADC



Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 18 of 25

CAD NOTE:

Place components on signals as close as possible to the FAN connectors, up to 1 inch.

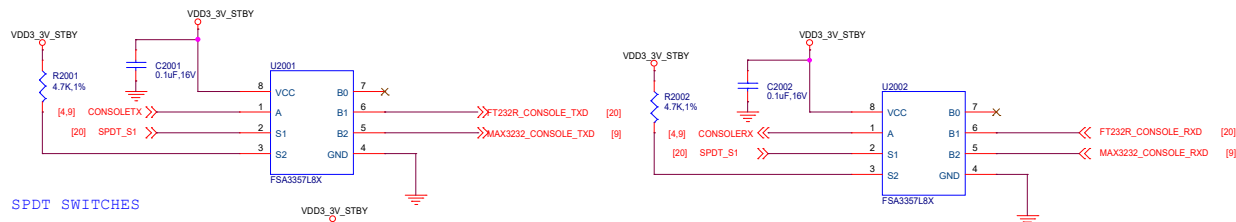


TACH, PWM

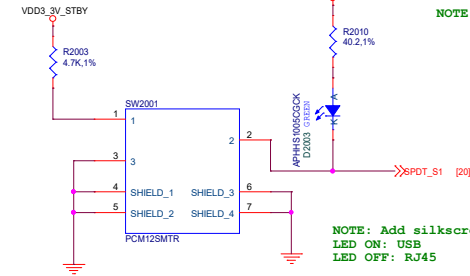


Size C	Document Number «Doc»	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 19 of 25

MUX/DEMUX SWITCHES



SPDT SWITCHES



NOTE: Add layout silkscreen to designate switch behaviour for U2001, U2002

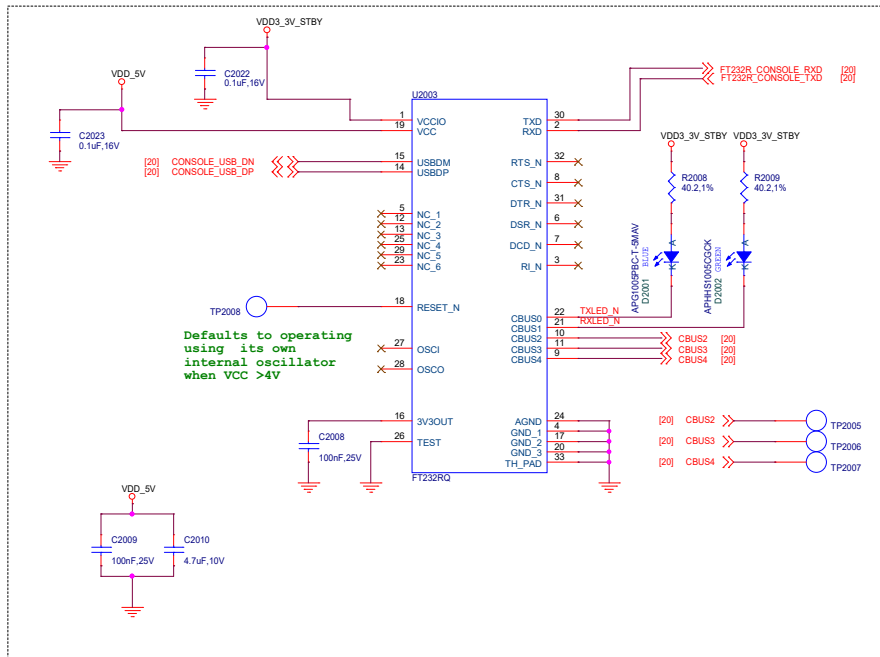
FSA3357 Functionality

S2	S1	Function
0	0	No Connection
0	1	B0 Connected to A
1	0	B1 Connected to A
1	1	B2 Connected to A

NOTE: Add silkscreen
LED ON: USB
LED OFF: RJ45

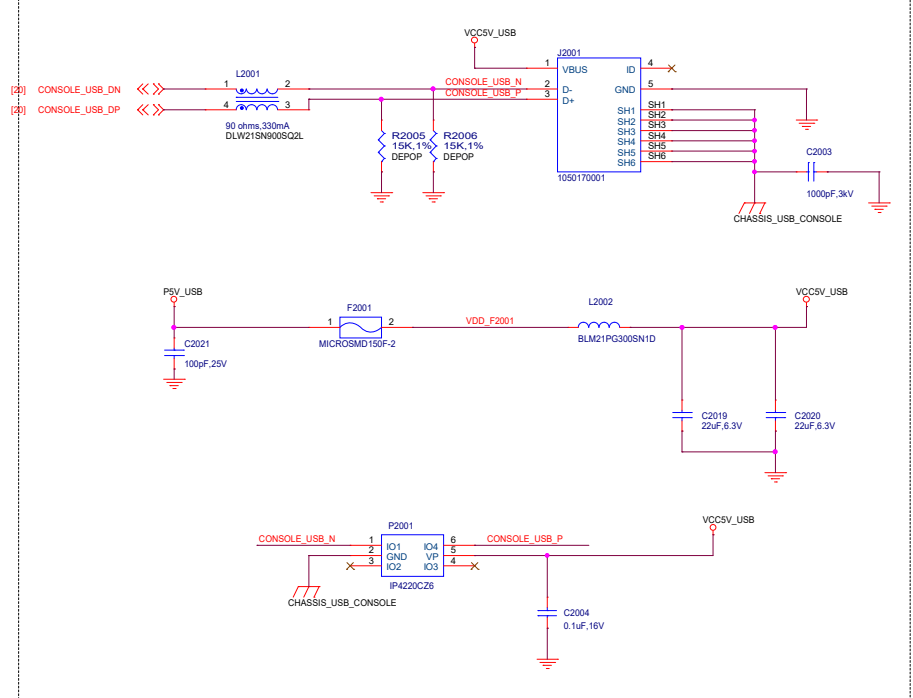
CONSOLE UART5

FT232R



Defaults to operating
using its own
internal oscillator
when VCC >4V

MICRO USB CONNECTOR

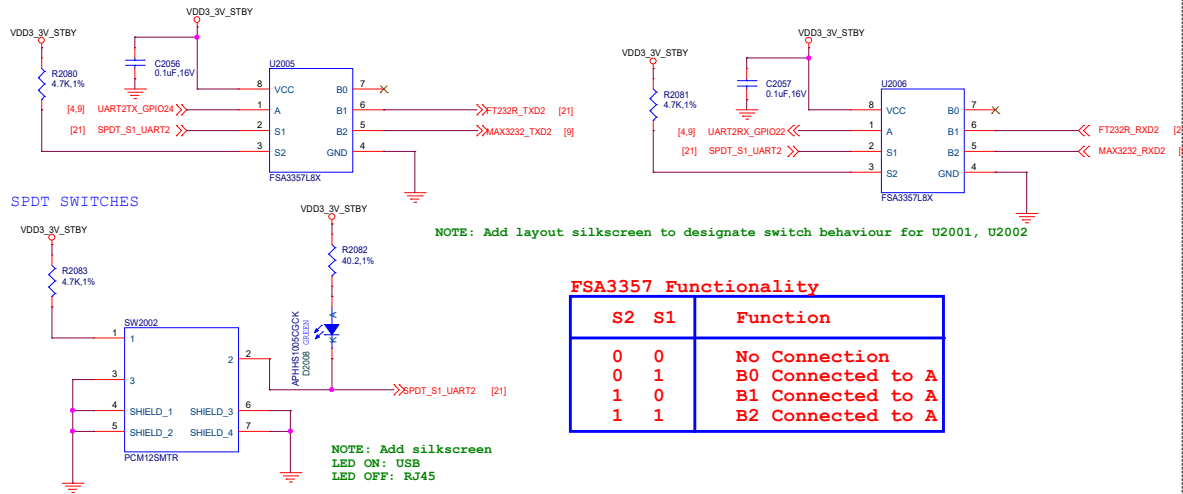


MUX/ DEMUX SWITCHES, FT232, USB CONN



UART2

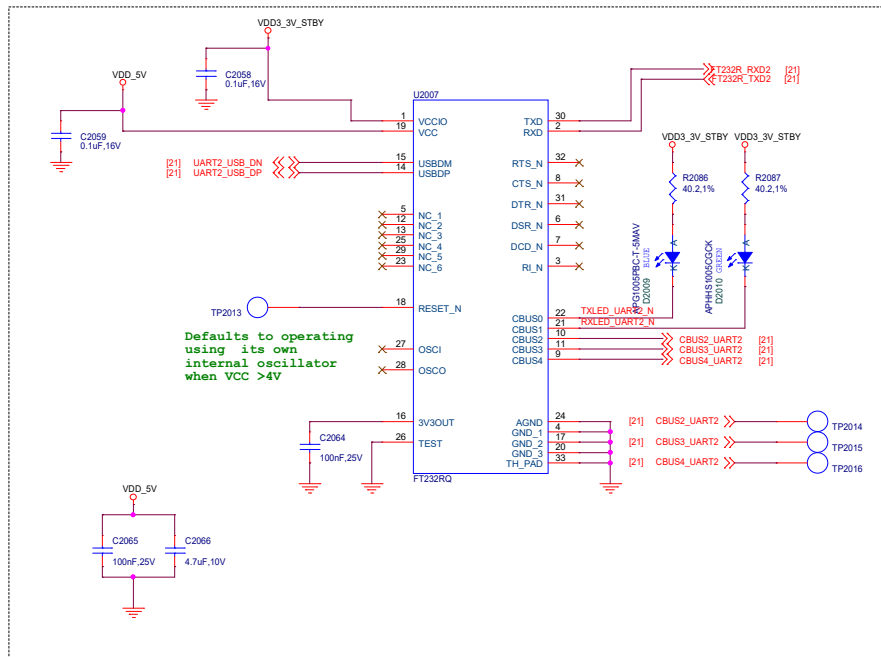
MUX/DEMUX SWITCHES



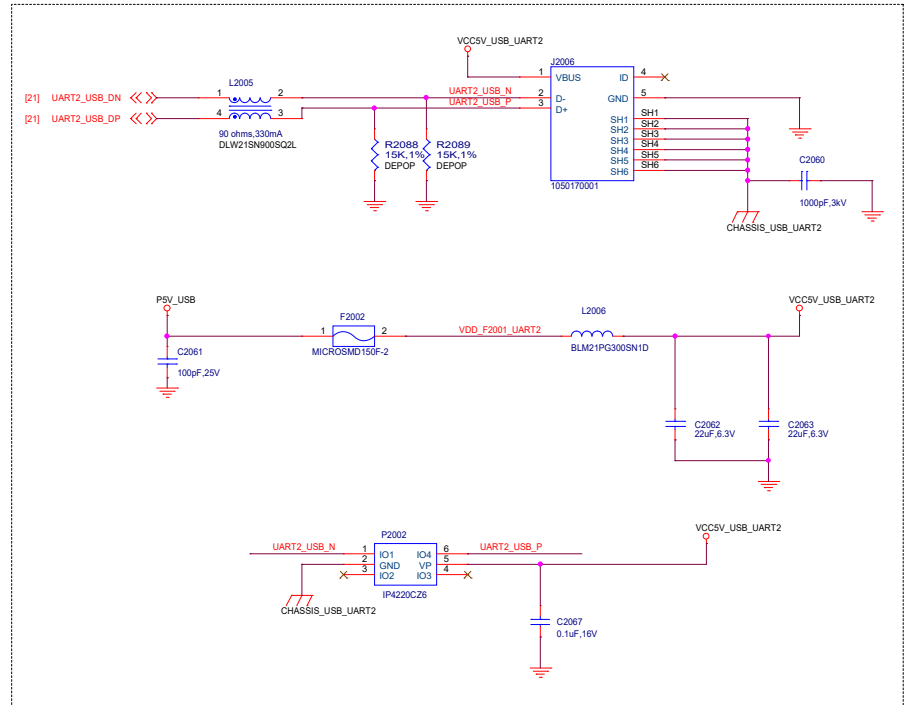
FSA3357 Functionality

S2	S1	Function
0	0	No Connection
0	1	B0 Connected to A
1	0	B1 Connected to A
1	1	B2 Connected to A

FT232R



MICRO USB CONNECTOR

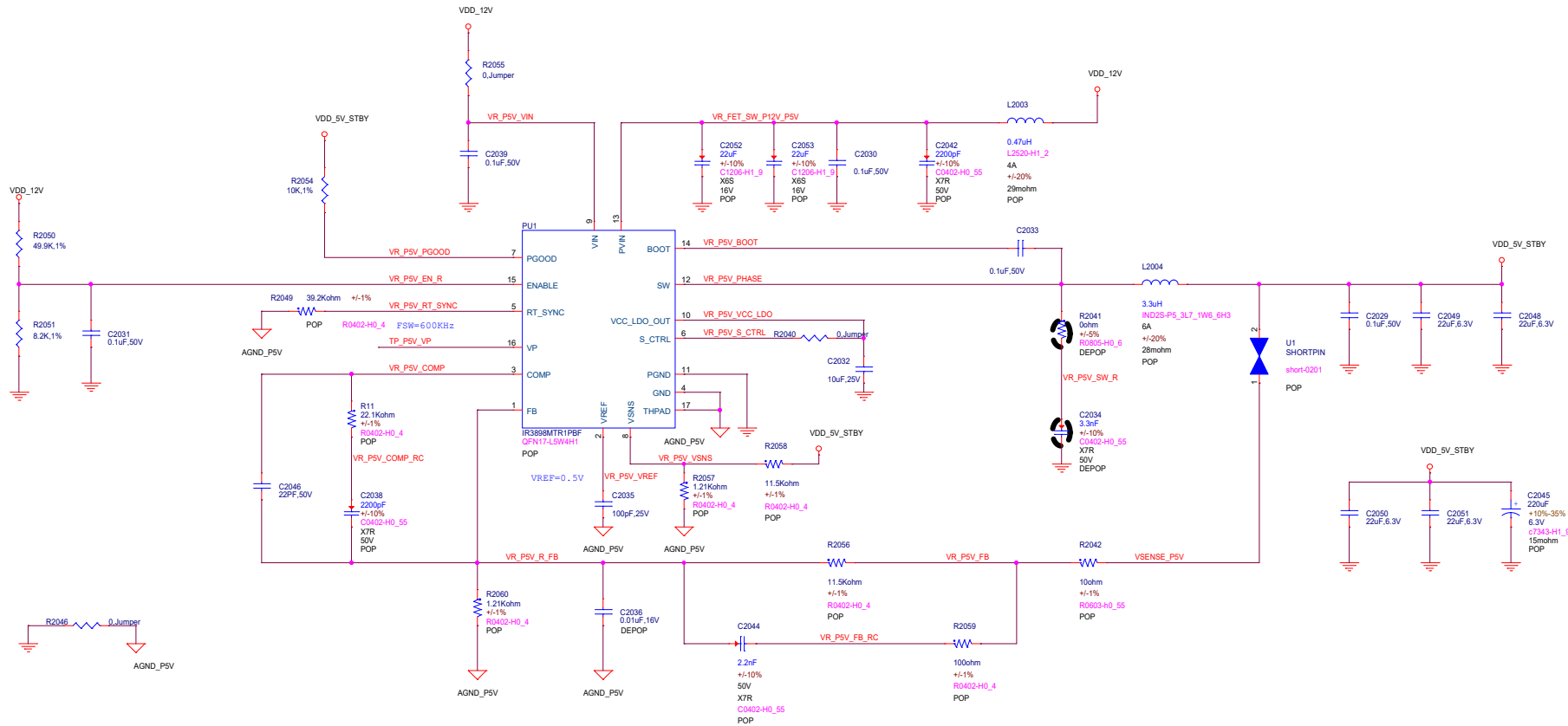


MUX/ DEMUX SWITCHES, FT232, USB CONN

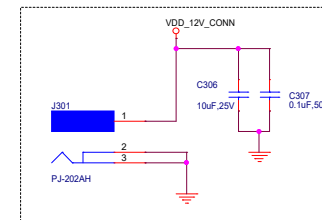


PS 5V

P5V VR Design Requirement	
VIN	12V
VOUT	5V
DC Tolerance	+/-2%
Ripple Tolerance	+/-2.5%
Total Tolerance	+/-4.5%
IccTDC	4A
IccPeak	4A
Icc Step	2A
Slew Rate	1A/us



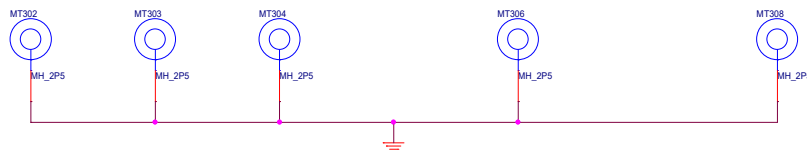
Barrel Connector 12V



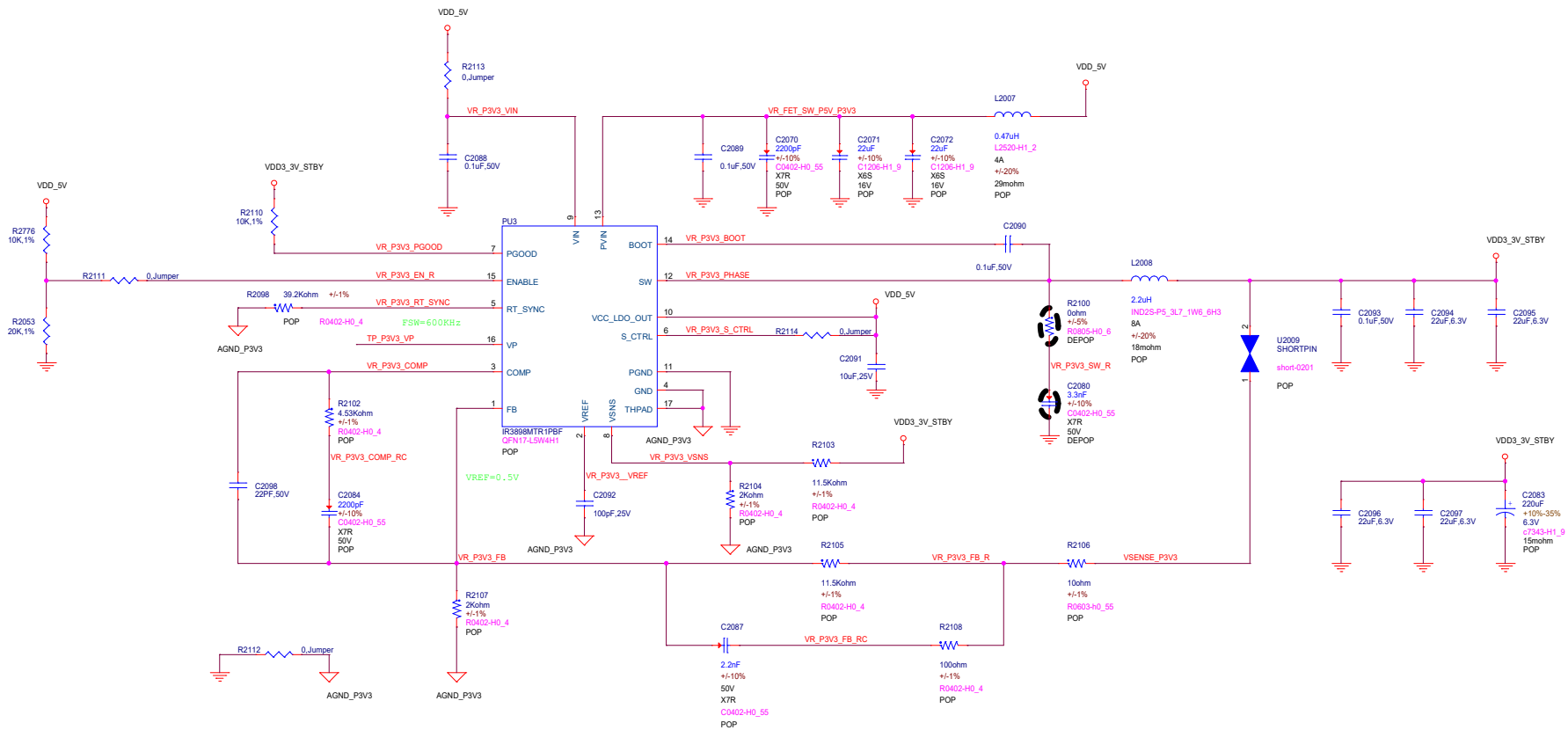
POWER 5V, 12V



Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 22 of 25



PS 3.3V



P3V3 VR Design Requirement

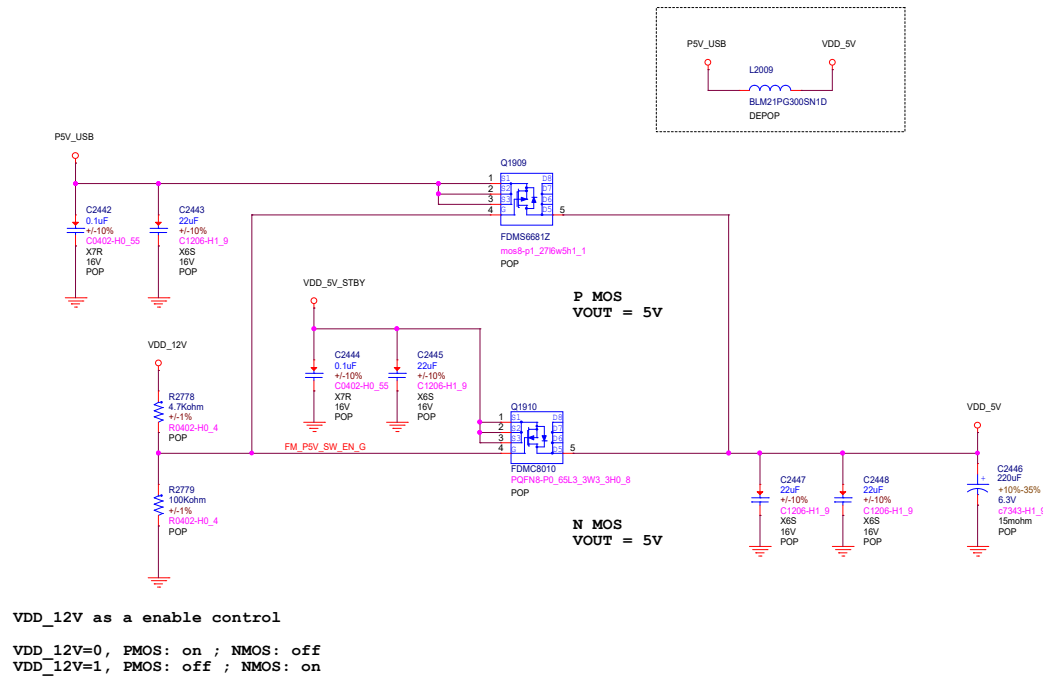
VIN	12V
VOUT	3.3V
DC Tolerance	+/-2%
Ripple Tolerance	+/-2.5%
Total Tolerance	+/-4.5%
IccTDC	4A
IccPeak	4A
Icc Step	2A
Slew Rate	1A/us

POWER 3.3V

Size C	Document Number <Doc>	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 23 of 25

VDD_5V POWER SWITCH

RESERVED FOR DEBUG USE



5V POWER SWITCH



Size C	Document Number «Doc»	Rev 0.11
Date:	Thursday, September 19, 2019	Sheet 24 of 25

REVISION HISTORY

Revision History - DVT

@2019/1/17

1. De-pop R1210/R1207/R1209, Place 150 Ohm termination on HS2500 module for DACG, DACR, and DACB signals
2. For solving PU1 OCP issue, add VDD_5V PS SWITCH, page 24
3. add a 3-pins header (J2010) for I2C13
4. remove J2003
5. add a test point on VDD_RGMII_REF

@2019/2/22

1. replace a MiniSASHD connector with the PCIe Edge connector

@2019/5/10

1. change the net name from KLUDGE_GPIO63 to CPU_RST#

@2019/8/15

1. change J1201 VGA connector to female connector

@2019/8/24

1. Page 11: Change text "From HS2500" to "From RunBMC Module"
2. Page 12: Change text "are placed on HS2500" to "are placed on RunBMC Module"
3. Change "MAX3232_RXD5" to: "MAX3232_CONSOLE_RXD"
4. Change "MAX3232_TXD5" to "MAX3232_CONSOLE_TXD"
5. Change "MAX_UART5_TX" to "MAX_CONSOLE_TX"
6. Change "MAX_UART5_RX" to "MAX_CONSOLE_RX"
7. Change "UART5_TX" to "CONSOLE_TX"
8. Change "UART5_RX" to "CONSOLE_RX"
9. Change "FT232R_RXD5" to "FT232R_CONSOLE_RXD"
10. Change "FT232R_TXD5" to "FT232R_CONSOLE_TXD"
11. Change "UART5_USB_DN" to "CONSOLE_USB_DN"
12. Change "UART5_USB_DP" to "CONSOLE_USB_DP"
13. Change "UART5_USB_N" to "CONSOLE_USB_N"
14. Change "UART5_USB_P" to "CONSOLE_USB_P"
15. Change "CHASSIS_USB_UART5" to "CHASSIS_USB_CONSOLE"

@2019/8/26

1. Page 1: change PCIe to "Edge Connector" instead of "MiniSAS HD Connector"

@2019/8/27

1. GPIO pin number change to match pinout v1.4

@2019/9/10

1. Correct the pin name for J1501A.59/J1501A.61

@2019/09/16

1. Remove Power Topology Diagram on Page 2 and leave it blank

@2019/09/19

1. Change PCIe Edge Connector to x4 instead of x16

Revision History

